Introduction to Semiconductor Manufacturing and FA Process

IPC Technical Seminar
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Course Objective

• Provide basic understanding on Semiconductor.
• Introduce semiconductor process flow from wafer fabrication to package assembly and final test, and what the semiconductor device failure analysis is and how it is conducted.
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SEMICONDUCTOR?
Basic Semiconductor
What is a Semiconductor?

- A **conductor** is a material which “conducts” electricity easily (such as metals).
- An **insulator** is a material which is a very poor conductor of electricity (such as glass).
- A **semiconductor** (silicon) is a material which acts like an insulator, but can behave like a conductor when it is combined with other materials.

“Semi + Conductor” or “半 + 導體”
Basic Semiconductor
Silicon in the environment

- Silicon is the seventh-most abundant element in the universe and the second-most abundant element on the planet, after oxygen.
- Silicon makes up about 25 percent of the Earth's crust.
- Silicon has good thermal conductivity.
Basic Semiconductor
Semiconductors in the Periodic System

Periodic Table of the Elements

IV semiconductors

III-V semiconductors
Basic Semiconductor
Silicon Crystalline Structure

• A crystal is a solid composed of atoms in a **SINGLE UNIFORM** array/structure.

• Each **silicon atom** is “connected” to its **four nearest neighboring silicon atoms**.

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  |   |   |   |   |   |   |   |   |   |
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Many atoms including silicon like to have **EIGHT** electrons in the ir outer “orbit”.

But, silicon only has **FOUR** outer electrons.

Solution: Bonding between two Si atoms by sharing 1 electron from each atom.
Basic Semiconductor
Bond Pictures of N-type & P-Type Silicon

- **N-Type**
  - Arsenic (As) and Phosphor (P) have 5 valence electrons
  - 1 additional electron can move through the crystal
  - Conduction

- **P-Type**
  - Boron (B) has 3 valence electrons
  - 1 electron is missing, a hole can move through the crystal
  - Conduction
Basic Semiconductor
Silicon Wafer Production Process

1. Polycrystalline Silicon

2. Crystal Growth

3. Single Crystal Silicon Ingot

4. Crystal Trimming and Grinding

5. Slicing

6. Edge Rounding

7. Lapping

8. Etching (Chemical Polishing)

9. Polishing

10. Cleaning

11. Inspection

12. Packing / Shipping

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Basic Semiconductor
Chronology of Silicon Wafer Size Increase

<table>
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<th>Wafer Size (mm)</th>
<th>Wafer Size (inch)</th>
<th>When (year)</th>
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<tr>
<td>150 mm</td>
<td>5.9 inch</td>
<td>1980</td>
</tr>
<tr>
<td>200 mm</td>
<td>7.9 inch</td>
<td>1991</td>
</tr>
<tr>
<td>300 mm</td>
<td>11.8 inch</td>
<td>2001</td>
</tr>
<tr>
<td>450 mm</td>
<td>18 inch</td>
<td>~2017</td>
</tr>
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Basic Semiconductor
Wafer Size Comparison: 200mm vs. 300mm

Number of chips per wafer: ~150%
Cost reduction per chip: ≥ 30%
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Semiconductor Supply Chain

- Wafer Fabrication (Front End)
- Assembly & Test (Back End)
- Customers
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Semiconductor Manufacturing Processes Overview
Front End Process (Wafer Fabrication)
Front End (FE) Process
Wafer Fabrication Process

- **Wafer Preparation**
- **Semiconductor Circuit Design**
- **Pattern Preparation**

- **Stepper Exposure**
- **Photoresist Coating**
- **Oxidation Layering**

- **Development**
- **Etching**
- **Ion Implantation**

- **Wafer Test**
- **Metallization**
- **Chemical Vapor Deposition**
Front End (FE) Process
Wafer Fabrication Processes
Front End (FE) Process
Cross section view of full process

Single Chip (Die)

Cross Section
Front End (FE) Process
Front End Process Line
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Back End Process (Assembly & Test)
The process of encasing a die (chip) in materials such as plastic or metal.
- Prevent physical damage and corrosion.
- Support the electrical contacts which connect the device to a circuit board.
- Dissipate heat produced in the device.
## Back End (BE) Process

### Package Variations

### Lead Frame Package
- **P-DSO 430mils** (Plastic Dual-in-line Small Outline)
- **P-DSO 300mils** (Plastic Dual-in-line Small Outline)
- **P-LCC** (Plastic Leaded Chip Carrier)
- **P-DIP** (Plastic Dual-In-line Package)
- **TSSOP** (Thin Shrink Small Outline Package)
- **MQFP** (Metric Quad Flat Package)
- **VQFN** (Very thin Quad Flat No lead)

### Laminate Package
- **PBGA** (Plastic Ball Grid Array)
- **SC70** (Small Outline Transistor)
- **SOT-23** (Small Outline Transistor)
- **DPAK** (Decawatt Package)

### Wafer Level Package
- **LFBGA** (Low Profile Fine-Pitch Ball Grid Array)
- **LFBGA** (Low Profile Fine-Pitch Ball Grid Array)
- **WLP** (Wafer Level Package)

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Back End (BE) Process
Back-End (Assembly and Test) Process

- **Wafer Back Grinding**
- **Wafer Mounting**
- **Wafer Sawing**
- **Die Attach**
- **Die Attach Cure**
- **Marking**
- **Lead Finish (Plating)**
- **Post Mold Cure (PMC)**
- **Molding**
- **Wire Bonding**
- **Trim/Form/S Ingulation**
- **Final Test**
- **Final Visual Inspection (FVI)**
- **Packing**
- **Shipping**

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Back End (BE) Process
Wafer Back Grinding

- The typical wafer supplied from ‘wafer fab’ is 600 to 750μm thick.
- Wafer thinned down to the required thickness, 50um to 75um, by abrasive grinding wheel.

› 1\textsuperscript{st} step : Use a large grit to coarsely grind the wafer and remove the bulk of the excess wafer thickness.
› 2\textsuperscript{nd} step : Use a finer grit to polish the wafer and to accurately grind the wafer to the required thickness.
Back End(BE) Process
Wafer Mounting

• Mount a wafer backside onto a sticky tape which is stretched onto a wafer frame for easy handling purpose during the wafer saw and die attach processes.

Sticky Tape for Wafer Mount (Blue tape)
Wafer Mount Frame
Back End(BE) Process
Wafer Sawing(Dicing Saw)

• Process by which individual silicon chips (die) are separated from each other on the wafer.
• Get the wafer cut per each lines with the D.I(De-ionized) water to prevent any electrostatic issue or contamination.
Back End (BE) Process
Die Attach (Die Bonding)

- Attach the die onto the lead frame by using the Epoxy adhesive or solder.

Epoxy or solder is dispensed in the die flag area of the lead frame in a specified pattern (usually star) followed by a pick and place process that removes the die from the tape carrier and places it over the dispensed epoxy.
Back End (BE) Process

Die Attach Cure

- Cure the die attach paste in order to harden it and to obtain its optimal mechanical and electrical properties.
- Products attached by glue is maintained at a temperature (usually about 125~175°C range) for a prolonged period of time.
Back End (BE) Process

Wire Bonding

- The electrical connection between die and lead frame with the use of the Gold, Copper, Aluminum wires.
Back End (BE) Process
Molding

- Encapsulate semiconductor die with the molding compounds (black plastic materials).
- Protect the device mechanically and environmentally from the outside environment like light, heat, humidity and dust.
Back End(BE) Process
Post Mold Cure(PMC)

- Ensure the mold compound is completely cured.
- Accelerate the curing process by rising temperature which can improve some material’s physical properties.
Back End(BE) Process
Lead Finish(Plating)

• Apply the coat of metal(Sn or SnPb) over the leads of package to connect mechanically and electrically between the package and the printed circuit board(PCB) and protect corrosion, abrasion and improve solderability.

• During the plating process the lead frame strip goes through a series of steps involving pretreatment, rinse, plating, drying, and inspection.
Back End (BE) Process

Marking

- Put identification, traceability, and distinguishing marks on the package.
- Either ink or laser methods are used to mark packages.
- Laser marking is preferred in many applications because of its higher throughput and better resolution.

[Laser Marking Machine]

IFX company name and logo
Device name
Date code
Lot Identification
**Back End (BE) Process**

**Trim/Form/Singulation**

- **Trim** - Cutting of the dampers that short the leads together.
- **Form** - Forming of the leads into the correct shape and position.
- **Singulation** - Individual units are singulated from the lead frame strip, inspect for lead coplanarity etc, and placed in trays or tubes.

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*Trim/Form/Singulation Machine*

*Trim/Form/Singulation Punch Die*
Back End (BE) Process
Final Test (Electrical Testing)

- Verify reliability of semiconductor by electrifying package to test its function at various levels of temperatures (Ambient, Hot and Cold).
- Electrical Testing is the process of segregating functionally good devices from the rejects.

Test Equipment

Bin 1: Good Quality Devices
Bin 2–4: Good Devices at Lower Performance Rating
Bin 5: Rejects from Contact tests failures
Bin 6: Rejects from Parametric test failures
Bin 7: Rejects from Functional test failures
Bin 8: Rejects from other test failures
Back End (BE) Process
Final Visual Inspection (FVI)

• Screen out the visual defects on the finalized semiconductor package with naked eyes, magnifier, microscope or equipment for visual inspection in order to ship only good parts to customers.
Back End (BE) Process
Packaging/Shipping/Delivery

- Pack the finished semiconductor products in the packaging materials like trays, tubes, reels, shipping box, container and finally deliver to the customer.
Back End (BE) Process
Cross section view of package

Cross section

Die Attach
Bond Wire
Die
Epoxy Mold Compound
Leadframe Pad
Lead
Front End (FE) Process
Back End Process Line
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What is Failure Analysis?

• Determine how or why a semiconductor device has failed.
• Analyze failed products and clarify the failure causes and mechanism, and provide feedback to the manufacturing and design process not only to prevent reoccurrence in the future and but also to improve manufacturing and product quality.
FA Process Flow
Non Destructive Analysis

Customer → Failure Analysis Request

Visual inspection
- Check Data (failure mode, product name, failure rate, photo, lot code, etc)
- Clarify package external defects like package cracks/chips, bent lead, broken lead, foreign material etc using microscope

Electrical Verification
- Curve tracer
- Bench test
- ATE (Automated Test Equipment)

X-ray inspection
- Verify the construction inside a sample like wire condition (sweeping wire, broken wire, sagging wire, short between wires etc), die attach voids, no die (chip), etc

SAT (Scanning Acoustic Tomography)
- Delamination at the interfaces of two distinct layers
FA Process Flow
Destructive Analysis

- De-Capsulation
  - Check the surface of die(chip) to clarify crack, chip, burnt mark etc

- Fault Localization
  - IR-LIT(Infrared-Lock In Thermography)
  - TIVA(Thermal Induced Voltage Alteration)
  - EMMI(Emission microscope)

- Die Level Analysis
  - Delayering, FIB(Focused Ion Beam)
  - SEM(Scanning Electron Microscope)
  - EDX(energy Dispersive X-ray)
  - RIE(Reactive-Ion Etching)

- Final Report
  - Customer
Part of your life. Part of tomorrow.