HITFET™ + Configurations

From fully featured to standard low-side

Scope and purpose

HITFET™ + devices propose various features compared to a standard low-side switch, including more pins for diagnostic signal to micro-controller, adjustable slew-rate for best trade-off between Electro Magnetic Interference (EMI) and power losses, high inrush current capability, active free-wheeling and very low leakage in OFF state. When some features are not needed, pin count can be reduced. This application note shows the recommended configurations.

Intended audience

This document is targeted for all electronics design engineers who need HITFET™ + low-side power switches in applications where pin count has to be kept minimal.

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2 BTS3xxxEJ recommended configurations

2.1 Pinout reminder

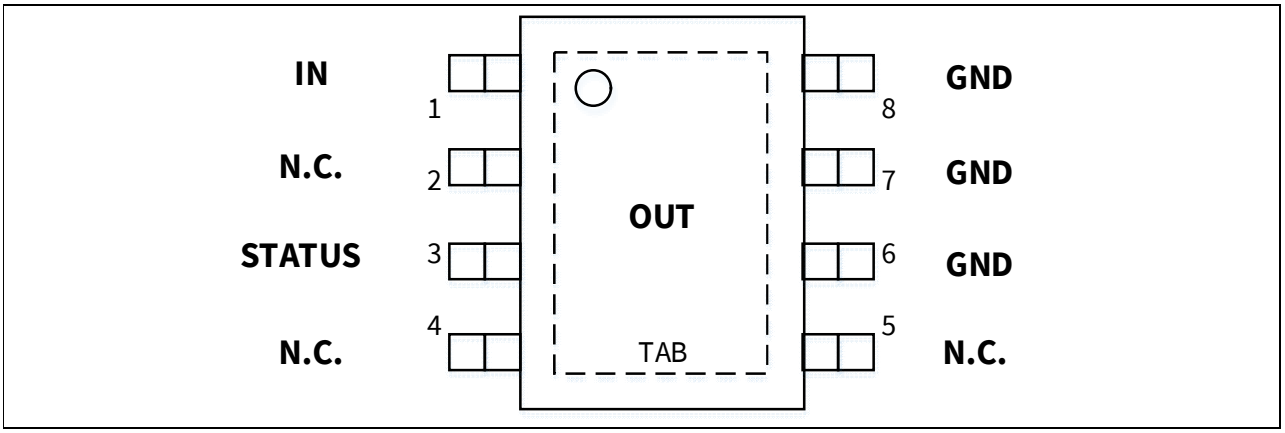


Figure 1 Pinout reminder

Table 1 Pin functionality reminder

Pin	Symbol	I/O	Function
1	IN	Input	“high”: switch ON the Power DMOS
			“low”: switch OFF the Power DMOS and reset the STATUS
2	-	-	Not connected
3	STATUS	Output	“high”: normal operation
			“low”: overtemperature condition, stays low until reset
4	-	-	Not connected
5	-	-	Not connected
6,7,8	GND	I/O	SOURCE of power DMOS and Logic, GND pins must be connected together
Cooling tab	OUT	I/O	DRAIN of power DMOS. Connected to Load.

2.2 Analysis of possible configurations

Infineon HITFET™ + BTS3xxxEJ family is easy to understand and straightforward to use.

If digital feedback is not needed in the application, then the STATUS pin can be left open with no drawback to BTS3xxxEJ family functionalities. It benefits from the smaller footprint of the TDSO-8 package compared to BTS3xxxTF the family.

Table 2 and Table 3 show an overview of the possible configurations.

Table 2 BTS3xxxEJ optimal configuration

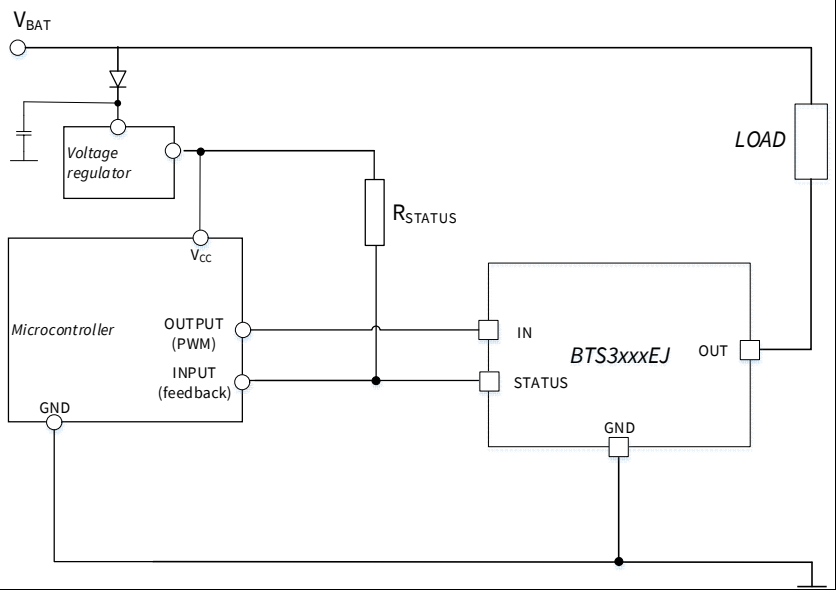
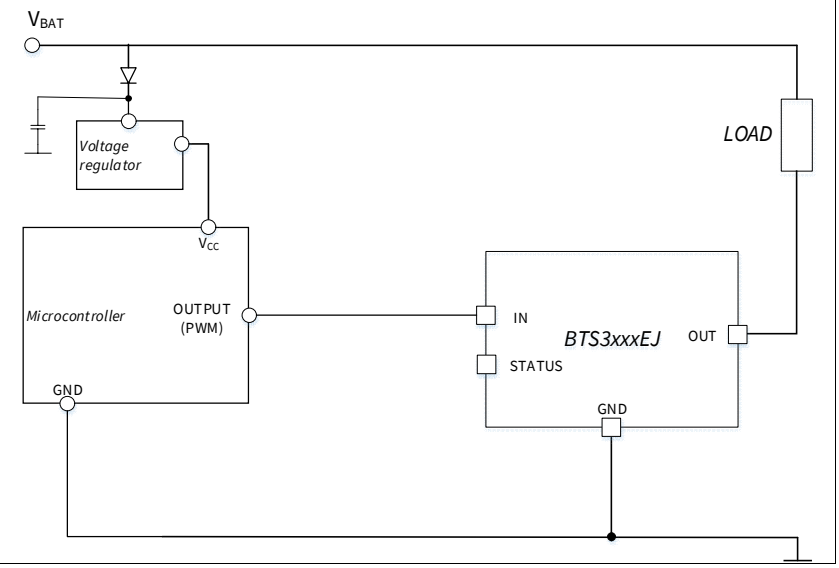
Fault feedback via STATUS pin	**Available,** reset by IN=low	

Table 3 BTS3xxxEJ one-pin configuration

Fault feedback via STATUS pin	**NO**	

3 BTF3xxxEJ recommended configurations

The BTF3xxxEJ fully featured family offers attractive features in a TDSO-8 package. However, all features may not be needed in the application, or the pin count matters because of limited number of available microcontroller pins.

In this case, some of the pins may or may not be used, depending on the feature needed.

3.1 Quick find page

This section gives an overview of the features that can be shed depending on customer needs and the number of available pins from microcontroller.

Table 4 takes you to the configuration that you need and can help you save pins of your microcontroller.

For full feature configuration see **Table 6**.

Table 4 Application requirements

No STATUS pin and no Fast PWM required	**Table 7**
$I_{LIM(TRIGGER)}$ is needed at each IN cycle and Slow PWM is enough*	**Table 8**
$I_{LIM(TRIGGER)}$ is needed at each IN cycle and Fast PWM is required*	**Table 9**
No need for lowest leakage while OFF (ENABLE pin)	**Table 10**
No STATUS, $I_{LIM(TRIGGER)}$ is needed at each IN cycle and Slow PWM is enough*	**Table 11**
No need for lowest leakage while OFF (ENABLE pin) and no need for STATUS pin	**Table 12**

* $I_{LIM(TRIGGER)}$ at each cycle may impact device lifetime. Refer to datasheet for values of $I_{LIM(TRIGGER)}$ and I_{LIM} depending on your device. Refer to your local sales contact or distributor for more information.

3.2 Pinout reminder

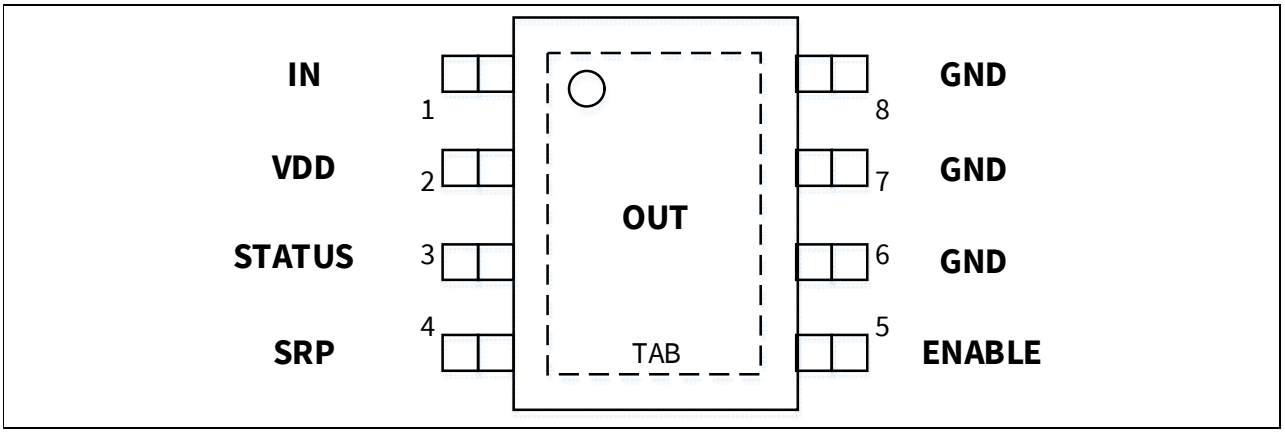


Figure 2 Pinout reminder

[There are several different “pinout reminder” sections and Figures. Add to each title what is specific about it for easy distinction.]

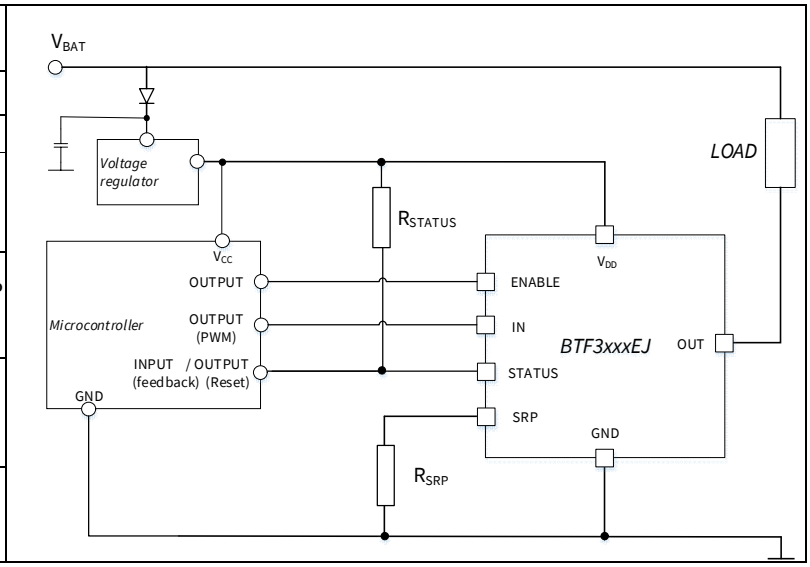
Table 5 Pin functionality reminder

Pin	Symbol	I/O	Function
1	IN	Input	“high”: switch ON the Power DMOS
			“low”: switch OFF the Power DMOS
			only if pin ENABLE is “high”
2	VDD	Input	Logic supply voltage, 3 V to 5.5 V
3	STATUS	Input	Reset of latches by microcontroller pull-up
		Output	“high”: normal operation
			“low”: overtemperature condition
4	SRP	Input	Slewrate control with external resistor
5	ENABLE	Input	“high”: IN pin enabled
			“low” IN pin disabled; leakage currents are minimum
6,7,8	GND	I/O	SOURCE of power DMOS and Logic, GND pins must be connected together
Cooling tab	OUT	I/O	DRAIN of power DMOS. Connected to load.

3.3 Full feature configuration analysis – 3 pins available on microcontroller

Table 6 Full feature configuration BTF3xxxEJ

Fault feedback via STATUS pin	**Available**
STATUS signal reset	**Possible**
$I_{LIM(TRIGGER)}$ reset	**Possible**
Timings as specified in datasheet	**YES**
Fast PWM possible	**YES,** with fast SRP pin configuration
Leakage min. in OFF state	**YES,** only when ENABLE=low
Active freewheeling	**Possible**



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3.4 Configurations when 2 pins from microcontroller available

Table 7 STATUS pin connected to GND

Fault feedback via STATUS pin	**NO**
STATUS signal reset	**NO**
$I_{LIM(TRIGGER)}$ reset	**Possible**, only by ENABLE=low
Timings as specified in datasheet	**YES**
Fast PWM possible	**YES,** with fast SRP configuration
Leakage min. in OFF state	**YES**, only when ENABLE=low
Active freewheeling	**Possible**

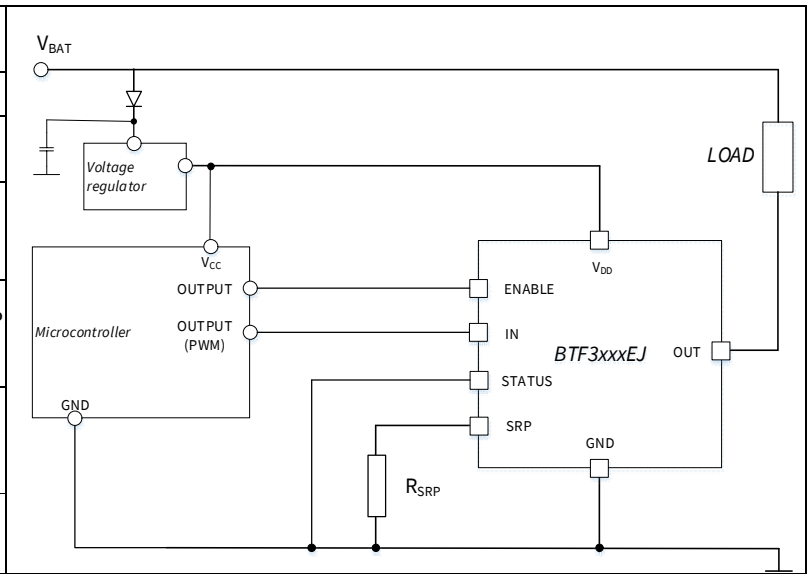

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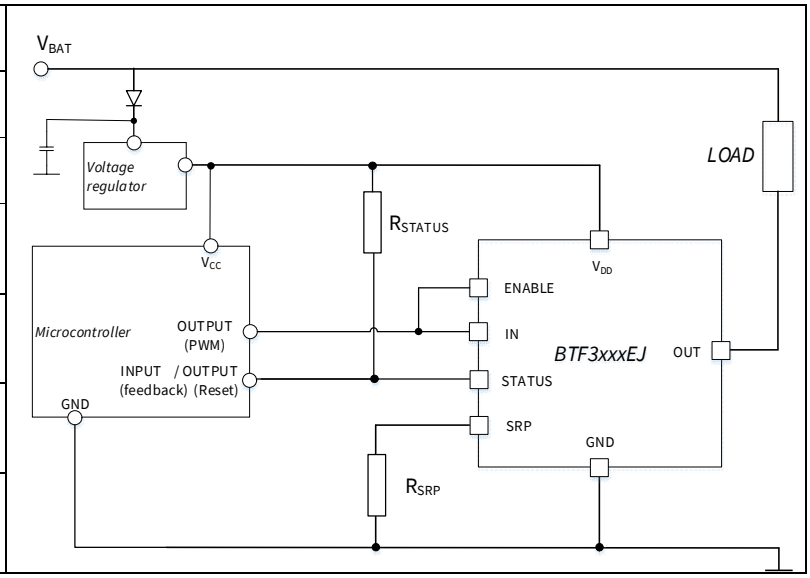
Table 8 IN pin and ENABLE pin connected together to microcontroller

Fault feedback via STATUS pin	**Available**
STATUS signal reset	**YES**, at each IN cycle[1)]
$I_{LIM(TRIGGER)}$ reset	**YES**, at each IN cycle[1)]
Timings as specified in datasheet	**NO**[2)]
Fast PWM possible	**Limited**[2)]
Leakage min. in OFF state	**YES**, only when ENABLE=low
Active freewheeling	**Possible**



1) Because IN pin and ENABLE pin are connected together, at each IN=ENABLE=" low", STATUS and $I_{LIM(TRIGGER)}$ are reset.

2) The turn-on is delayed at each cycle by $t_{ENABLE(MASKING)}$. Refer to parameter in datasheet for more information.
The turn-off can be considered as in fast SRP pin configuration.

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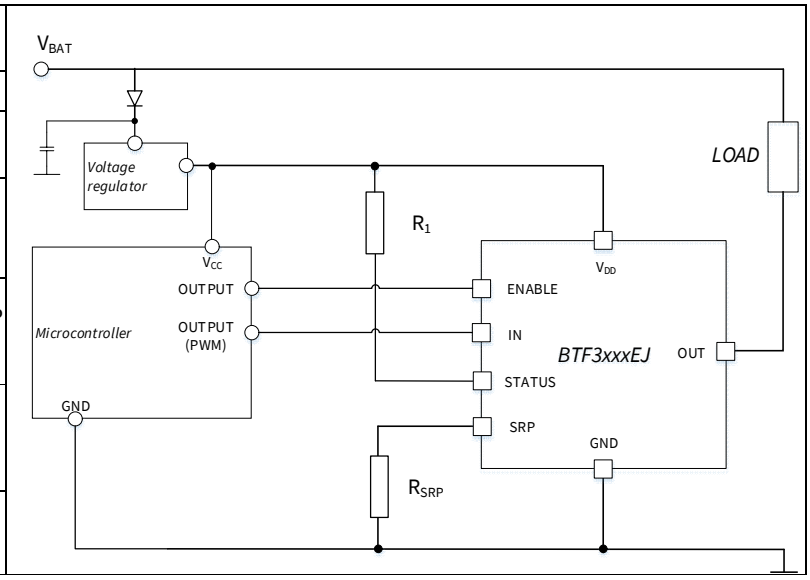
BTF3xxxEJ recommended configurations

Table 9 STATUS pin permanently pulled-up to V_{DD}

Fault feedback via STATUS pin	**NO**
STATUS signal reset	**Permanent**[1)]
$I_{LIM(TRIGGER)}$ reset	**YES**, at each IN cycle[1)]
Timings as specified in datasheet	**YES**
Fast PWM possible	**YES,** with fast SRP pin configuration
Leakage min. in OFF state	**YES**, only when ENABLE=low
Active freewheeling	**Possible**



1) Reset by ENABLE= “low” is not applicable since STATUS is reset permanently and $I_{LIM(TRIGGER)}$ is reset at each INPUT= “low” by the STATUS pin pulled-up to V_{DD} with the R_1 resistor. R_1=220 Ω for V_{DD}=5 V and R_1=100 Ω for V_{DD}=3.3 V. See **Figure 4** for details on the STATUS pin structure.

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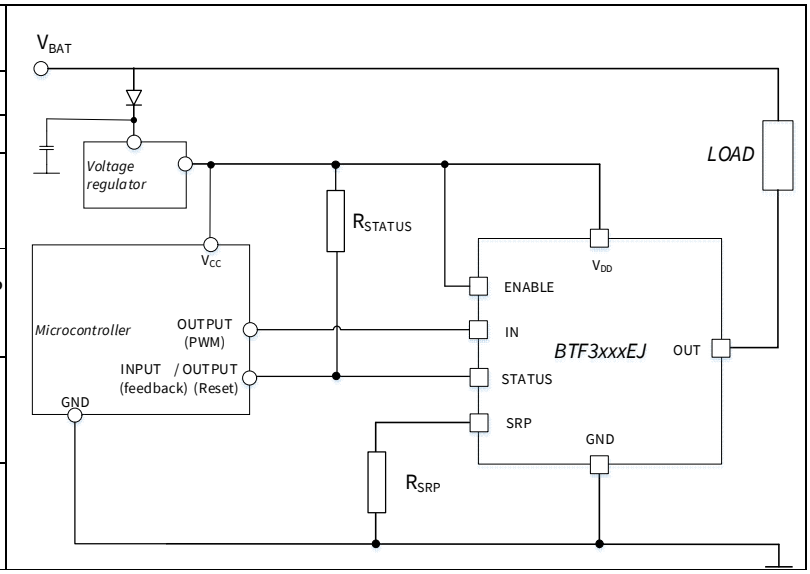
Table 10 ENABLE pin permanently connected to V_{DD}

Fault feedback via STATUS pin	**Available**
STATUS signal reset	**Possible**
$I_{LIM(TRIGGER)}$ reset	**Possible**
Timings as specified in datasheet	**YES**
Fast PWM possible	**YES,** with fast SRP pin configuration
Leakage min. in OFF state	**NO**[1)]
Active freewheeling	**Possible**



1) The leakage current on V_{DD} pin is $I_{DD(ON)}$. Refer to datasheet for values. It will not be acceptable in most automotive applications, where leakages in OFF state are critical, but can be accepted for non-automotive applications. The only advantage of this configuration over BTS3xxxEJ family is its fast PWM capability.

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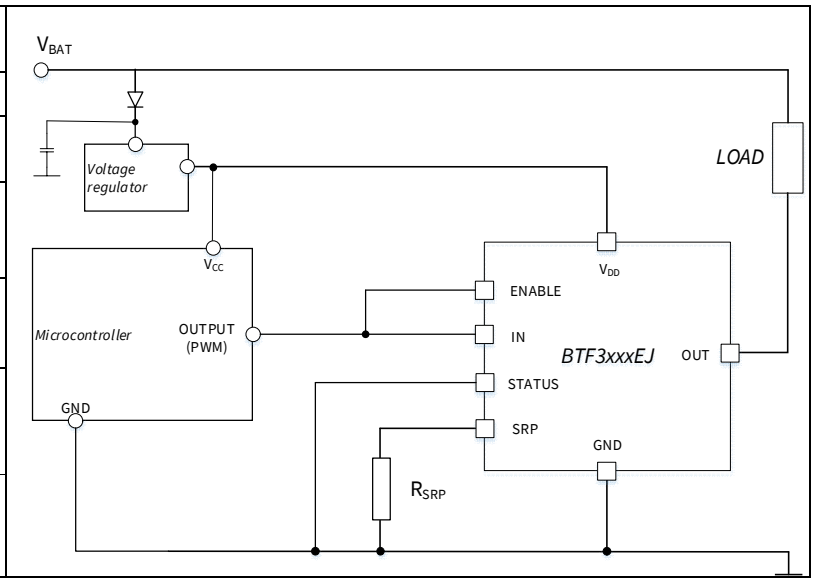
3.5 Configurations when only 1 pin from microcontroller is available

Table 11 IN pin and ENABLE pin connected together and STATUS pin connected to GND

Fault feedback via STATUS pin	**NO**
STATUS signal reset	**NO**
$I_{LIM(TRIGGER)}$ reset	**YES**, at each IN cycle[1)]
Timings as specified in datasheet	**NO**[2)]
Fast PWM possible	**Limited**[2)]
Leakage min. in OFF state	**YES**, only when ENABLE=low
Active freewheeling	**Possible**



1) Because IN pin and ENABLE pin are connected together, at each IN=ENABLE= “low”, $I_{LIM(TRIGGER)}$ is reset.

2) The turn-on is delayed at each cycle by $t_{ENABLE(MASKING)}$. Refer to parameter in datasheet for more information.
The turn-off can be considered as in fast SRP pin configuration.

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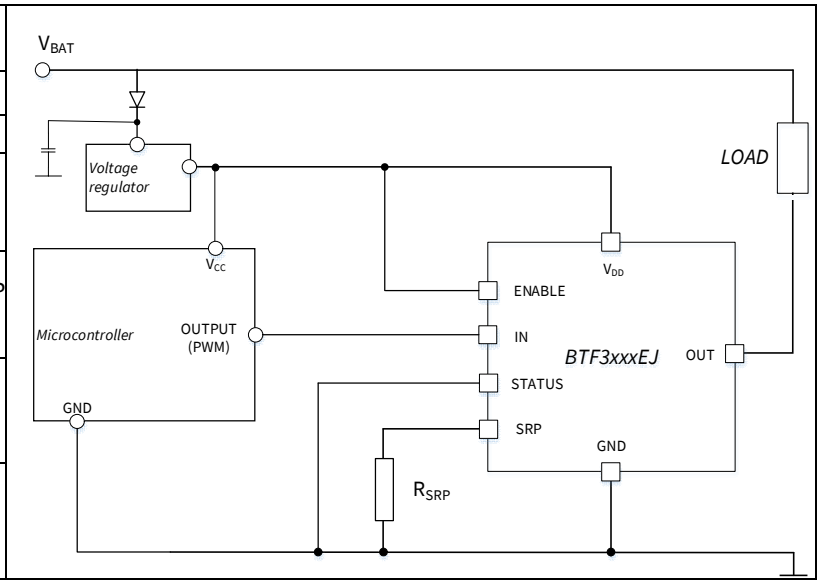
BTF3xxxEJ recommended configurations

Table 12 ENABLE pin permanently connected to V_{DD} and STATUS pin connected to GND

Fault feedback via STATUS pin	**NO**
STATUS signal reset	**NO**
$I_{LIM(TRIGGER)}$ reset	**NO**
Timings as specified in datasheet	**YES**
Fast PWM possible	**YES,** with fast SRP pin configuration
Leakage min. in OFF state	**NO**[1)]
Active freewheeling	**Possible**



1) The leakage current on V_{DD} pin is $I_{DD(ON)}$. Refer to datasheet for values. It will not be acceptable in most automotive applications, where leakages in OFF state are critical, but can be accepted for non-automotive applications. The only advantage of this configuration over BTS3xxxEJ family is its fast PWM capability.

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4 BTS3011TE recommended configurations

This chapter describes possible configurations for BTS3011TE.

4.1 Pinout reminder

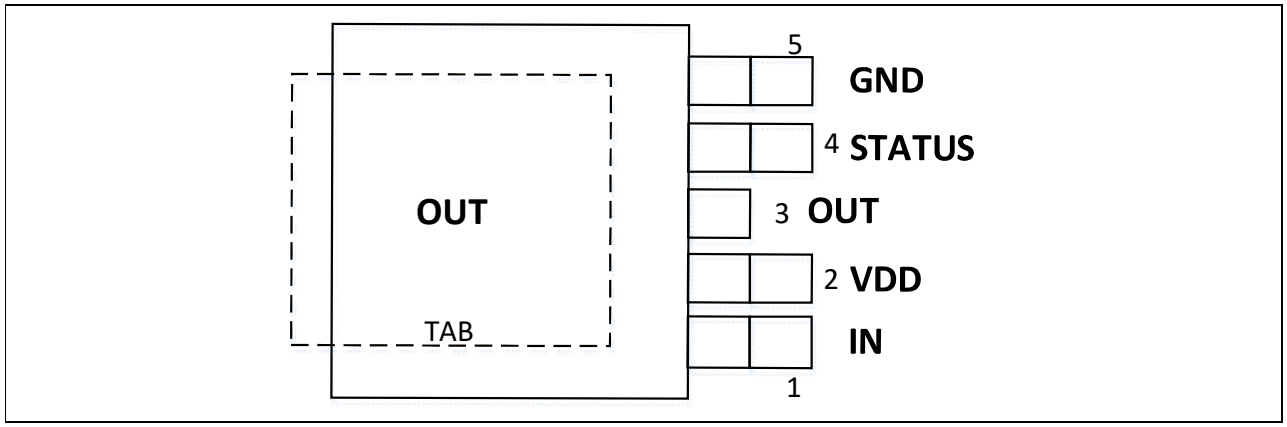


Figure 3 Pinout reminder

Table 13 Pin functionality reminder

Pin	Symbol	I/O	Function
1	IN	Input	“high”: switch ON the Power DMOS
			“low”: switch OFF the Power DMOS
2	VDD	Input	Logic supply voltage, 3 V to 5.5 V
4	STATUS	Input	Reset of latches by microcontroller pull-up
		Output	“high”: normal operation
			“low”: overtemperature condition
5	GND	I/O	SOURCE of power DMOS and Logic
Cooling tab, 3	OUT	I/O	DRAIN of power DMOS. Connected to Load.

4.2 Analysis of possible configurations

Table 14 Full feature configuration

Fault feedback via STATUS pin	**Available**
STATUS signal reset	**Possible**
$I_{LIM(TRIGGER)}$ reset	**Possible**
Timings as specified in datasheet	**YES**
Active freewheeling	**Possible**

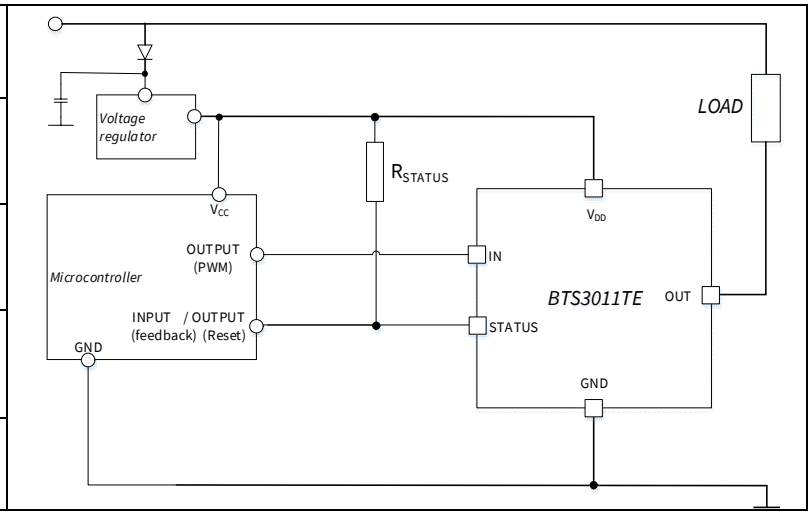
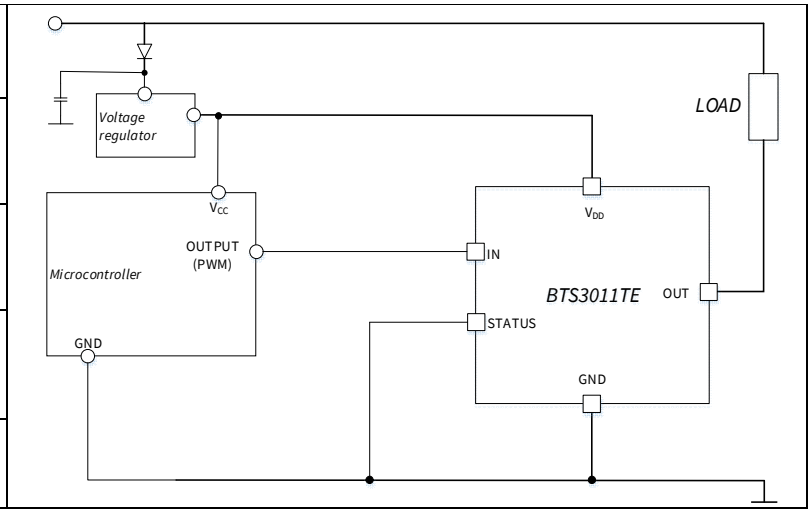


Table 15 STATUS connected to GND

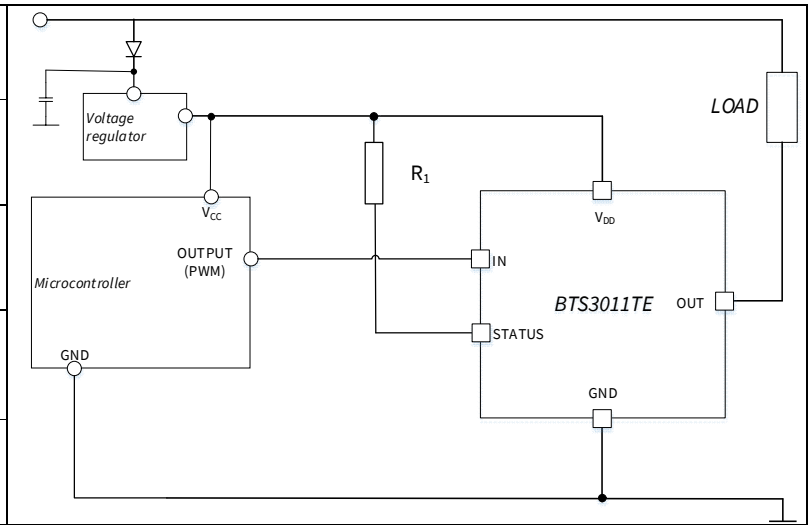
Fault feedback via STATUS pin	**NO**
STATUS signal reset	**NO**
$I_{LIM(TRIGGER)}$ reset	**NO**[1)]
Timings as specified in datasheet	**YES**
Active freewheeling	**Possible**



1) $I_{LIM(TRIGGER)}$ is available until first OT, then the current is limited to I_{LIM}, until V_{DD} is switched off and on again. Refer to datasheet for values.

Table 16 STATUS permanently pulled-up to V_{DD}

Fault feedback via STATUS pin	**NO**
STATUS signal reset	**Permanent**
$I_{LIM(TRIGGER)}$ reset	**YES**, at each IN cycle[1)]
Timings as specified in datasheet	**YES**
Active freewheeling	**Possible**



1) $I_{LIM(TRIGGER)}$ at each cycle may impact device lifetime. Refer to datasheet for values of $I_{LIM(TRIGGER)}$ and I_{LIM}. Refer to your local sales contact or distributor for more information. R_I=600 Ω for V_{DD}=5 V and R_I=100 Ω for V_{DD}=3.3 V. See **Figure 5** for details on the STATUS pin structure. Refer to your local sales contact or distributor for more information.

5 Appendix

5.1 BTF3xxxEJ STATUS pin diagram

In order to keep STATUS and $I_{LIM(TRIGGER)}$ permanently reset, the STATUS pin needs a pull-up resistor R_1 to V_{DD} with a value different from the R_{STATUS} resistor. During an overtemperature (OT) event or a dynamic temperature (ΔT) event, R_1 ensures that the voltage on the STATUS pin remains above the $V_{STATUS(RESET)}$ threshold. Additionally, the STATUS pin must receive an $I_{STATUS(RESET)}$ current as specified in order to provide sufficient current for reset. Refer to datasheet for values.

Figure 4 shows a schematic diagram of the internal structure of the STATUS pin for all HITFET™ + BTF3xxxEJ. The values from the diagram can be used to compute the appropriate resistor-based customer's V_{DD} voltage.

R_1=220 Ω can be used for V_{DD}=5 V

R_1=100 Ω can be used for V_{DD}=3.3 V

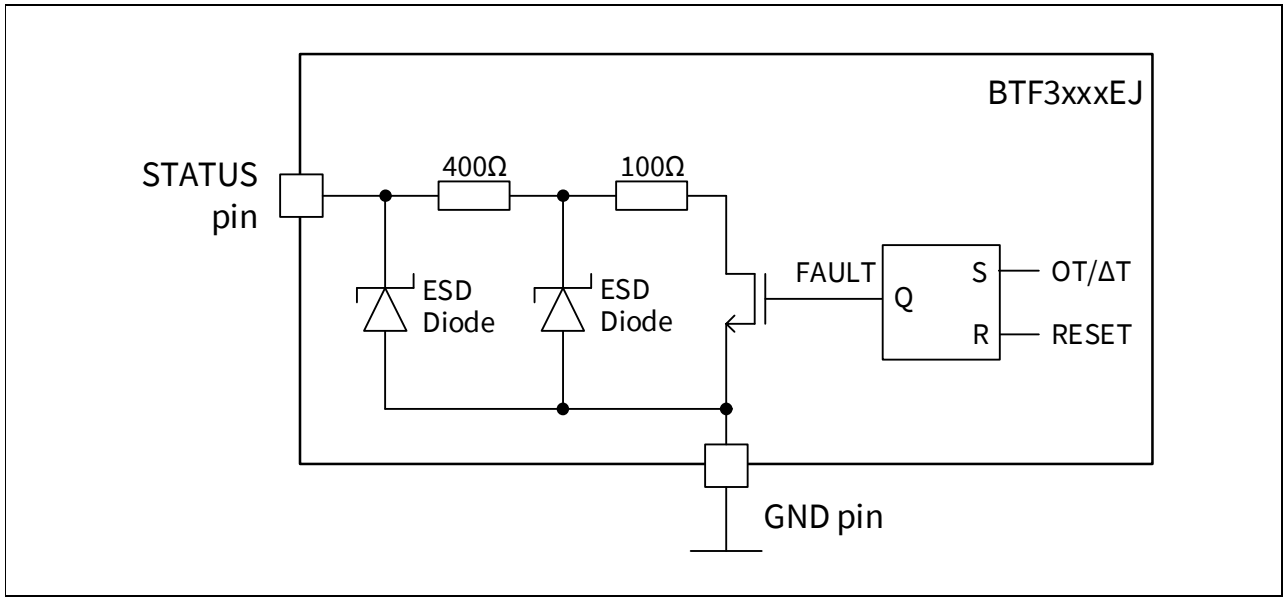


Figure 4 BTF3xxxEJ STATUS pin structure (typical values)

See **BTF3xxxEJ recommended configurations**.

5.2 BTS3011TE STATUS pin diagram

In order to keep STATUS and $I_{LIM(TRIGGER)}$ permanently reset, the STATUS pin needs a pull-up resistor R_1 to V_{DD} with a value different from the R_{STATUS} resistor. During an overtemperature (OT) event or a dynamic temperature (ΔT) event, R_1 ensures that the voltage on the STATUS pin remains above the $V_{STATUS(RESET)}$ threshold. Additionally, the STATUS pin must receive an $I_{STATUS(RESET)}$ current as specified in order to provide sufficient current for reset. Refer to datasheet for values.

Figure 5 shows a schematic diagram of the internal structure of the STATUS pin for HITFET™ + BTS3011TE. The values from the diagram can be used to compute the appropriate resistor-based customer's V_{DD} voltage.

R_1=600Ω can be used for V_{DD}=5V

R_1=100Ω can be used for V_{DD}=3.3V

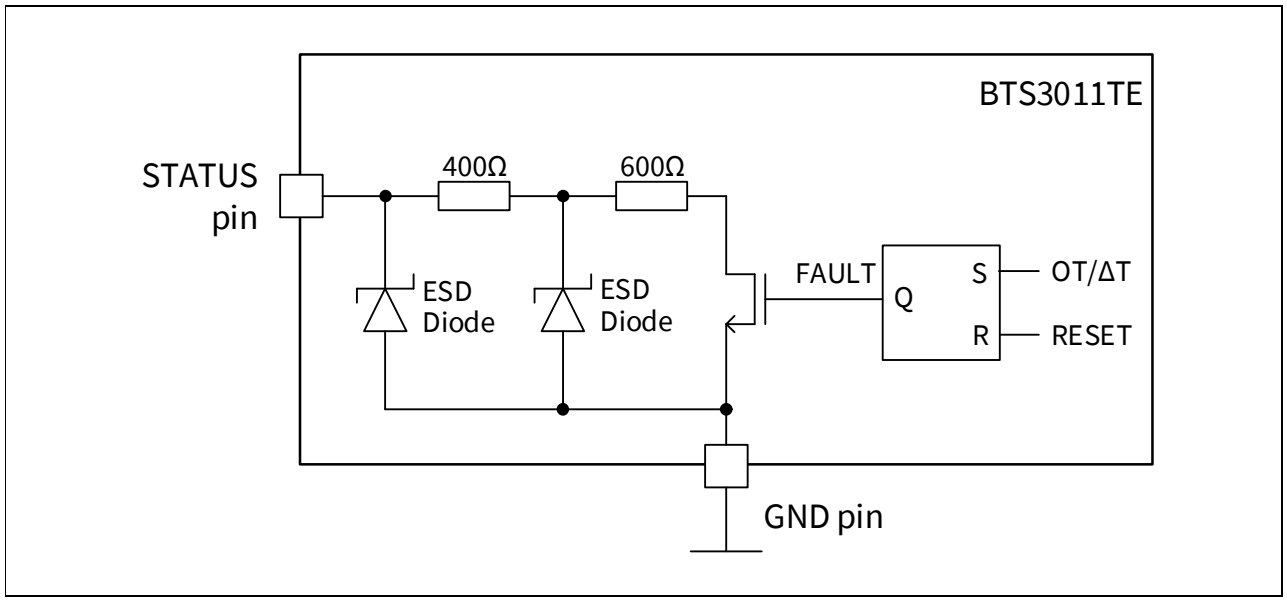


Figure 5 BTS3011TE STATUS pin structure (typical values)

See **BTS3011TE recommended configurations**.

6 Revision history

Major changes since the last revision

Revision	Date	Description of change
Revision 1.1	2021-03-08	Add Trade Mark on HITFET™ words
Revision 1.0	2018-09-08	Initial release

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