TLE6365 – PCB Layout and EMC Filtering

DC-DC Buck Converter with Reset

Z8F52274259

Application Note

Rev. 1.01, 2015-04-23

Automotive Power

Table of Contents

1 Abstract

This Application Note presents the application circuit and associated circuit layout for the DC-DC converter TLE6365. The TLE6365 is a buck converter with an integrated DMOS switching transistor and with an external free-wheeling diode that supplies an output voltage of 5 V with an output current of up to 1.2 A, converted from an input voltage range of 8 V to 32 V. The circuit is a recommendation of how to comply with automotive EMC requirements. Typical EMC measurement results are documented.

This document describes:

- PCB layout measures
- dimensioning of EMC filters

2 Introduction

Increased use of electronics in leads to a growing demand of auxiliary voltages such as 5 V for powering microcontrollers and digital circuitry. The efficiency of linear regulators normally used for this purpose is low, especially at higher load currents and at large input/output voltage differences. Furthermore they experience difficulties dissipating the heat produced, in particular since the permissible total power loss in electronic control units is limited. This accounts for the increasing use of DC-DC converters. These are capable of a highly efficient operation over a wide input voltage range. On the other hand DC-DC converters inevitably generate electromagnetic interference emissions by their switching behaviour. These emissions must to be reduced to a permissible minimum. At the same time system reliability must be ensured in the electromagnetic conditions in an automobile with being exposed to interference and disturbing pulses.

The application circuit presented in this document was tested in terms of its electromagnetic compatibility according to the following standards:

- CISPR 25
- IEC 62132-4
- ISO 7637

The measuring methods and limits of electromagnetic emission in a frequency range from 150 kHz to 1 GHz are defined in CISPR 25. The conducted electromagnetic emission from the TLE6365 was determined between 150 kHz and 110 MHz with the aid of an artificial network simulating a typical power network in vehicles. The test method described in IEC 62132-4, where RF power in the frequency range from 150 kHz to 1 GHz is coupled on a pin-selective basis, was used to determine the RF interference immunity of the TLE6365. Immunity to conducted disturbance was tested according to ISO 7637, which specifies methods for the injection of disturbing pulses typical for automobiles as well as functional ratings of the application under these conditions.

3 DC-DC Converter Application

3.1 Application Circuit

The application circuit recommended for proper operation of the TLE6365 is shown in **Figure 1**. Various external components are located at the pins of the TLE6365 for providing protection functions, determining of the operating range and serving as power storage. **Figure 1** lists the components with their recommended values.

A characteristic feature of DC-DC converter operation is the generation of electromagnetic emission at harmonics of the operating frequency, occurring when transistor and diode are switched. Rapid changes in current and voltage (di/dt, du/dt) and the block-shaped current drawn from the supply network cause high-frequency disturbance current and voltage that spread on a line-conducted basis through the surrounding area or through capacitive or inductive coupling. The spread of disturbance is also influenced by the input and output circuitry, i.e. by the choice of external components used. The characteristics of external circuitry of the TLE6365 and its effects require special attention.

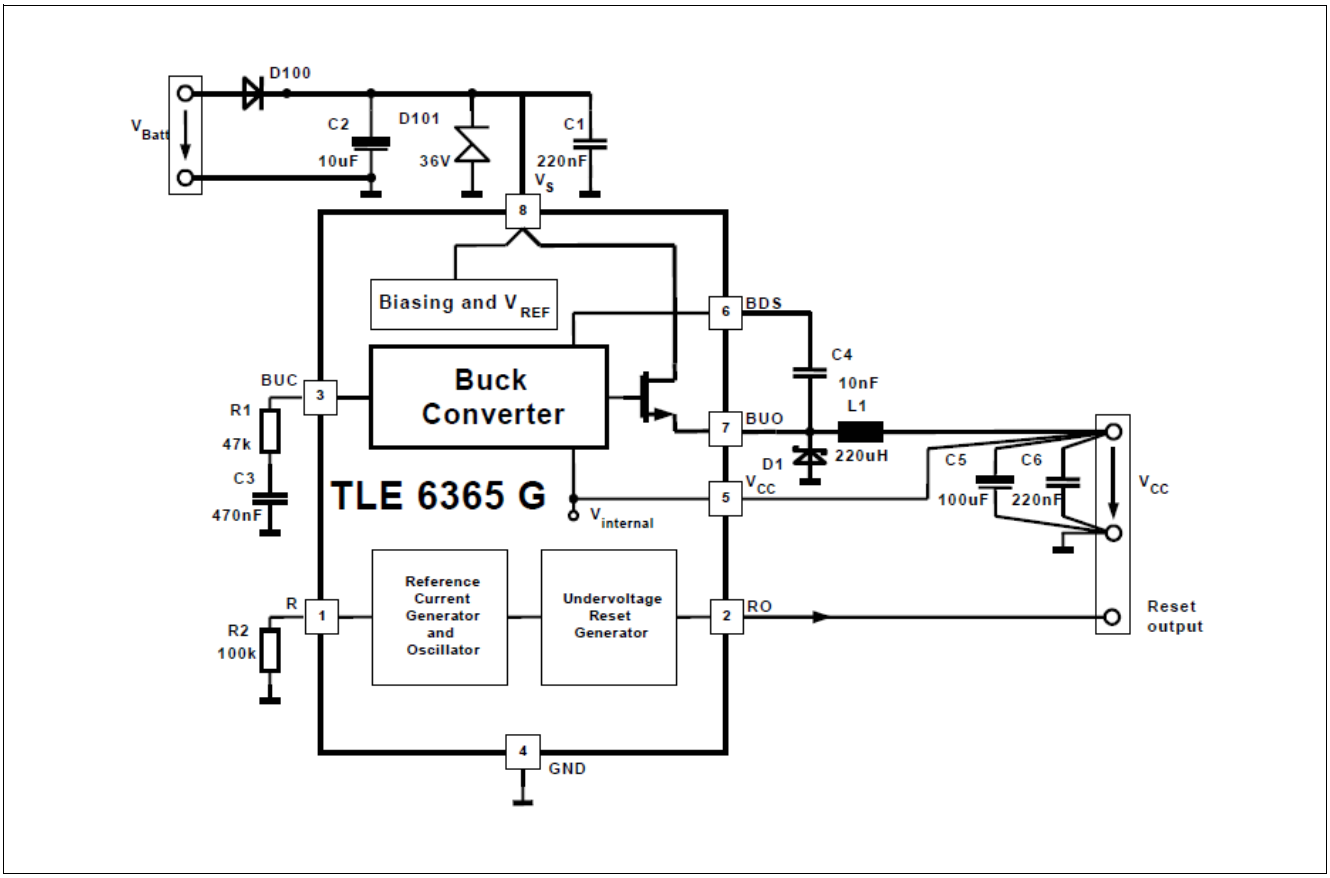

Figure 1 Application Circuit Diagram

Table 1 Bill of Materials: Application Circuit TLE6365

Part	Value	Remark
C1	220 nF	Ceramic SMD
C2	10 µF/22 µF	low ESR, e.g. EPCOS SpeedPower
C3	470 nF	
C4	10 nF	
C5	100 µF	low ESR, e.g.EPCOS SpeedPower
C6	220 nF	Ceramic SMD
D1	SS14	Schottky
D100	ES1B	Polarity protection diode
D101	36 V	Zener
L1	220 µH	Power choke
R1	47 kΩ	
R2	100 kΩ	Switching frequency: 50 kHz

3.1.1 Input Circuit – Pin VS

Two capacitors (C1, C2) are provided for the input circuit on the supply voltage pin VS. They stabilize the voltage and should be placed to the IC. The parallel circuit of C1 and C2 must have a low equivalent series resistance (ESR) so that the disturbing emission can be attenuated across a wide frequency range, from the 50 kHz operating frequency to the top MHz range. Tantalum low ESR capacitor types such as the SpeedPower series from EPCOS are therefore especially suitable for C1. Ceramic SMD capacitors with X7R dielectric are recommended for C2.

Increasing the capacitance of capacitor C1 from the 10 µF rating in the data sheet to 22 µF will improve emission behavior at V_{BATT}.

Diode D100 serves as reverse polarity protection. A Schottky diode is advantageous, if the circuit is dimensioned for maximum efficiency, as Schottky diodes have low forward voltage and hence they cause low power loss. A Zener diode (D101) is necessary for clipping overvoltage spikes. The diodes also protect the electrolytic capacitors and the IC from pulses occurring on an automobile's electrical distribution system.

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

3.1.2 Output Circuit – Pin BUO

Pin BUO is the switch output of the internal DMOS of the TLE6365. A freewheeling diode, the choke (L1) and the output capacitors (C5, C6) are connected to it. Using a Schottky diode (D1) is recommended in order to minimize diode forward conduction loss. The power choke rating should be at least 220 µH to ensure stable operation. The choke should also have low parasitic capacitance or a high series resonance frequency to minimize capacitive recharging currents. It is strongly recommended to use low ESR types for the output capacitors C5 and C6 of the buck converter. **Figure 2** shows the output voltage ripple of the TLE6365 with different output capacitors. The ripple is approximately 100 mV with a wired 100 µF standard electrolytic

capacitor. Using a 100 µF SMD Tantalum capacitor reduces the ripple to about 20 mV. As a rule, ceramic capacitors are especially suitable for high-frequency stabilizing. C6 should therefore be a ceramic capacitor with a X7R dielectric.

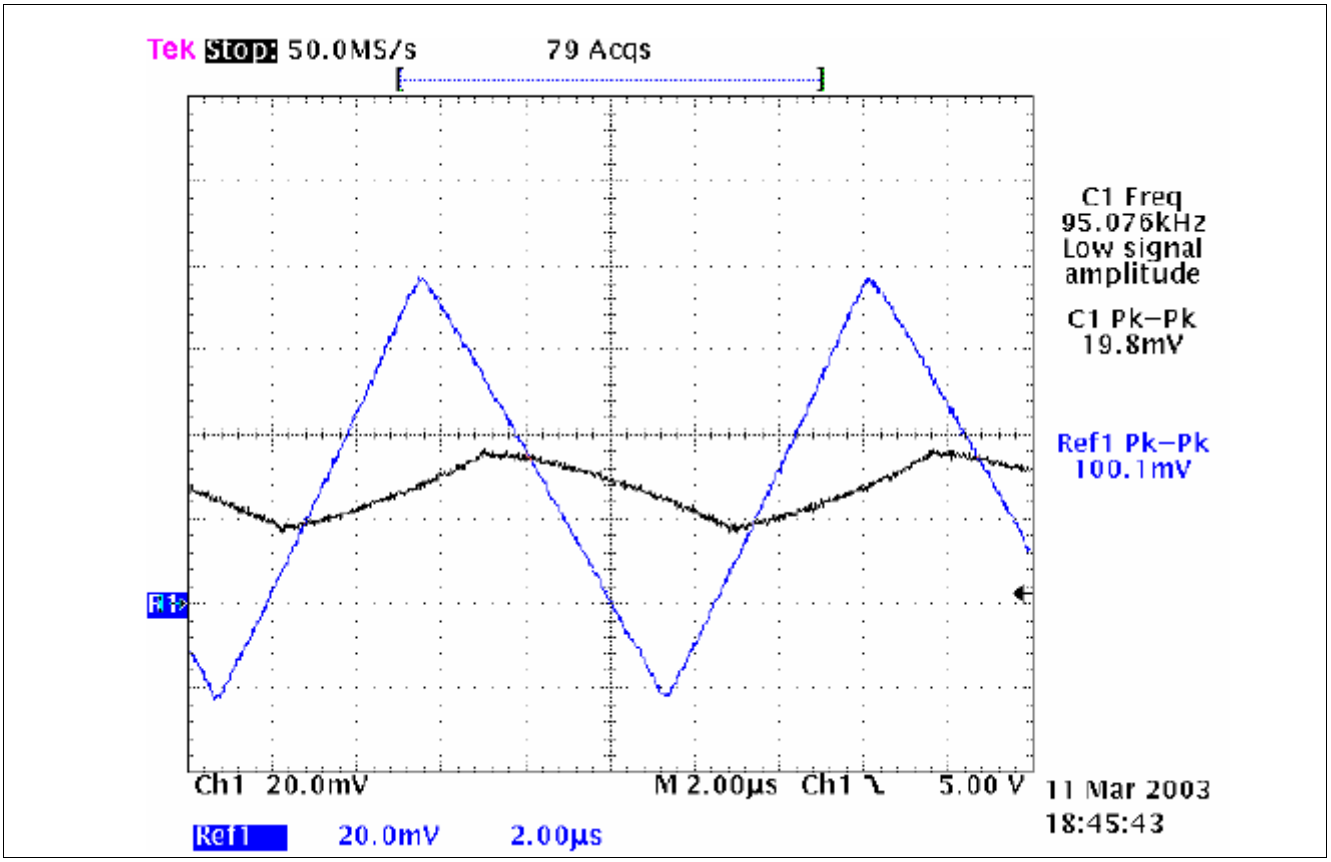

Figure 2 Ripple at the Output with Different Smoothing Capacitors

3.1.3 Buck Driver Supply – Pin BDS

Pin BDS supplies the DMOS gate driver inside the chip and must be equipped with a ceramic capacitor C4 = 10 nF.

3.1.4 Buck Converter Compensation – Pin BUC

The RC time delay element on pin BUC stabilizes the control of the buck converter.

The time constant $\tau = R1 \times C3$ can be changed by component matching in case of uneven switching time.

3.1.5 Reference Input – Pin R

The operating frequency of the DC-DC converter is set to 50 kHz by the external resistor R2 = 100 kΩ on pin R.

3.2 Layout Recommendations

As during component selection, parasitic effects must be considered when the layout is designed to minimize the spread of electromagnetic emissions and the components have to be connected in an optimal manner. For designing circuit layout the following aspects shown in **Table 2** must be taken into account:

Table 2 Layout Recommendations 1-9

Number	Recommendation
1	Circuit: input capacitor (C1/C2), switching transistor (T) and free wheeling diode (D1) should be as compact (low inductive) as possible.
2	The area of connection of T - L1 - D1, on which the switched voltage occurs, should be as small (low capacitive) as possible.
3	C1, C2, C5 and C6 should have short (low inductive) connections.
4	Forced routing of RF currents: The supply voltage should be routed via the pins of C1 and C2 and the output voltage should be routed via the pins of C5 and C6.
5	A shielding GND plane should be added underneath the DC-DC circuit.
6	The GND connection of C1, C2, D1, C5 and C6 should be designed as a common GND point with a direct via to the shielding GND- plane.
7	The GND connection of the IC should be made directly to the ground area.
8	A separate ground system should be provided for the DC-DC circuit by designing the connection to the external ground via only one track.
9	The ground connection of the application circuit should be of star shaped design to the network which provides the supply and to the network which is supplied. Ground looping can induce disturbance.

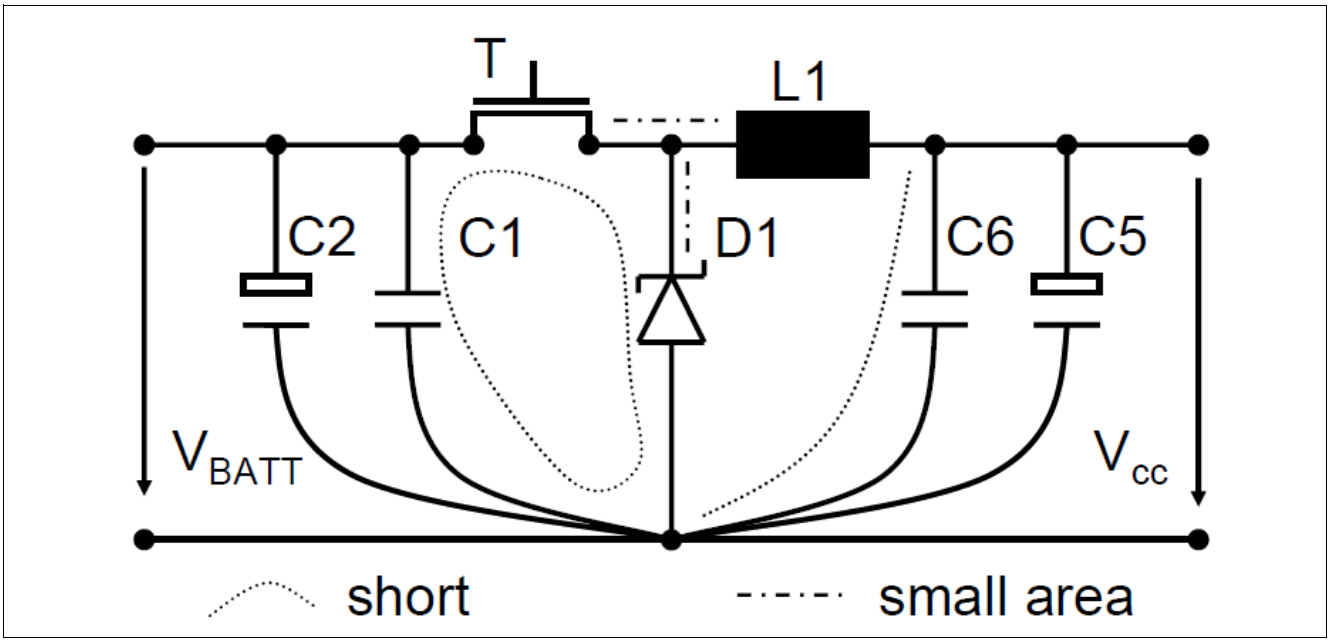

Figure 3 Optimizing the Circuit of a Buck Converter

3.3 Application Layout

This section shows how the above layout recommendations can be turned to practical count. **Figure 4** shows the section of the board taken up by the functional application circuit of the TLE6365 without protective diodes (D100 and D101).

The circuit was developed in a way that all components are located on the top layer of a 2-layer PCB. The bottom side of the board is a shielding reference ground area. **Figure 4** shows that the electrical circuit C1 – T – D1 is kept as small as possible (see **Table 2**, Recommendation 2). The track with the fast alternating voltage (high du/dt) on the switching transistor output is also as small as possible. This minimizes capacitive coupling. Capacitors C1, C2, C5, C6 and D1 are connected on a low-inductance basis (Recommendation 3) to a common GND point on the top layer, which only connects the GND layer on the bottom side of the board at a single point via plated-through holes (Recommendation 6). This prevents high-frequency high currents (high di/dt) of the switching cycles from flowing via the shielding GND area.

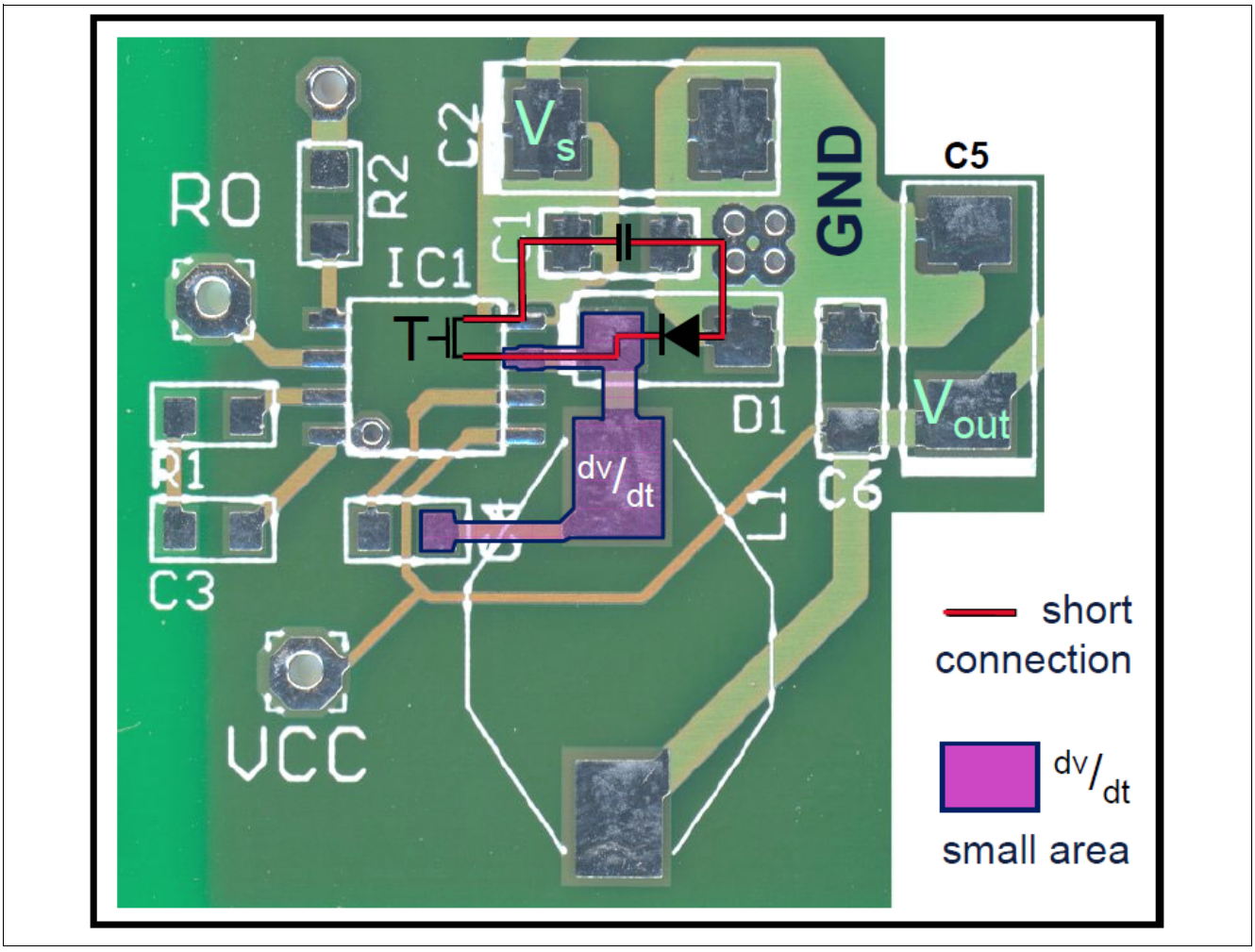

Figure 4 Example of Implementing the Layout Rules

4 RF Filtering

4.1 EMC Application Circuit

If emission is higher than permitted in the target application despite the above measures, additional EMC filters are required. The layout recommendations given in **Section 4.2** should also be taken into account. Otherwise there could be a negative impact on the attenuating effect of the filter network.

Depending on the requirements of the application, additional EMC filter components can be used in the input circuit to pin VS and in the output circuit to the 5 V terminal. A 15 µH choke in the supply line and a 4.7 µF capacitor from V_{BATT} to GND are recommended for input filtering to comply with CISPR 25 Class 5 emission limits. These components are shown in **Figure 5** as C100 and L100 in the input filter circuit. Together with capacitor C2 they form a π-filter.

If the same requirements apply to the output, it is recommended to employ a similar filter configuration consisting of a 2.2 µH choke (L200) in the V_{OUT} line and two capacitors with 47 µF and 47 nF (C201, C200) from V_{OUT} to GND. Capacitor C201 rated at 47µF forms part of the output capacitor in order to maintain the dynamic current-carrying capacity of the output voltage. The output capacitance is divided equally between the output smoothing capacitor (C5) and output filter capacitor (C201).

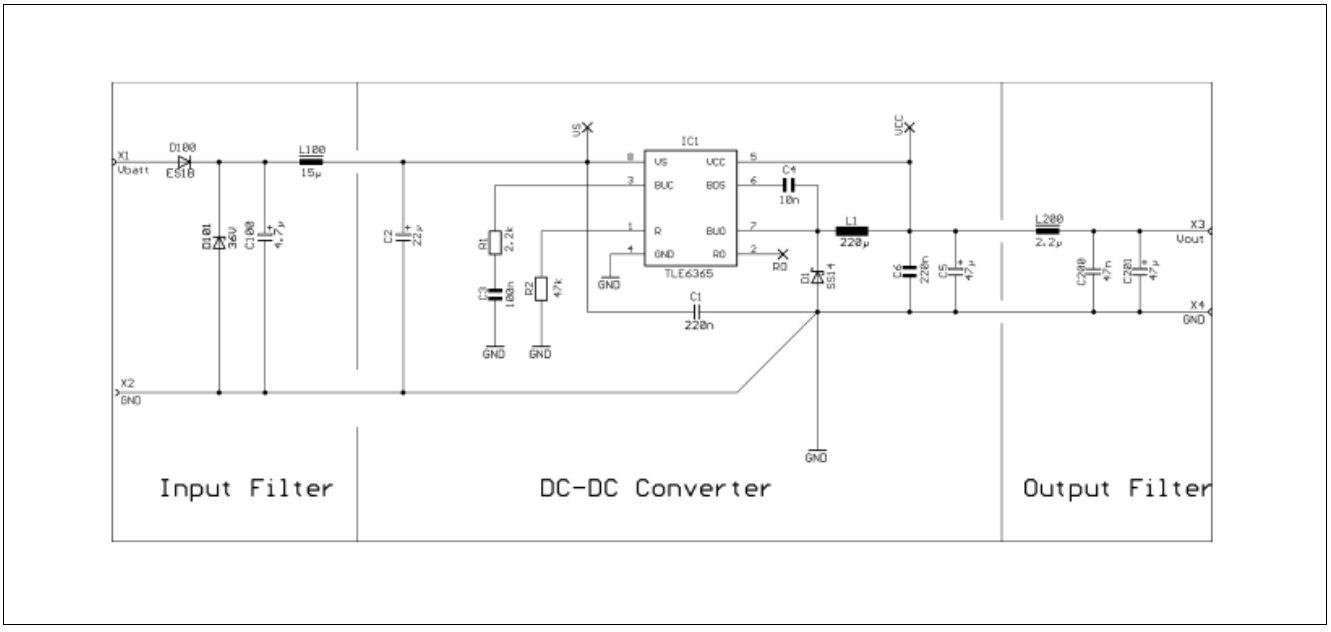

Figure 5 Circuit Diagram of the TLE6365 Reference Network with Input and Output Filter

The filter circuit at the output has no influence on the spread of disturbance at the input. This means only the input filter has to be equipped if only the emissions on the input side Vs are to be reduced. For reverse polarity protection and overvoltage protection, diodes (D100, D101) are located in before of the input filter. Circuit design must consider voltage drop on the chokes caused by the DC resistance of the chokes, during full-load operation. It is not recommended connecting feedback pin V_{CC} of the DC-DC converter for regulating the output voltage to V_{OUT} after filter choke L200. Tests show that this would increase emission and decrease control stability.

The components listed in **Table 3** are dimensioned for an output load of 3 W. They will not be overloaded in case of a short circuit at the output detected by the TLE6365.

Table 3 Component List of the EMC Application Circuit

	Part	Value	Package	Remark
Minimum equipment recommended	C1	220 nF	1206	X7R
	C2	22 µF	7243	low ESR, e.g. EPCOS SpeedPower
	C3	1000 nF	1206	
	C4	10 nF	0805	
	C5	47 µF[1)]/100 µF[2)]	7243	low ESR
	C6	220 nF	1206	X7R e.g. EPCOS SpeedPower
	D1	SS14	DO-214AC	Schottky
	D100		DO-214AC	Reverse Polarity protection
	D101	ZD 36 V	DO-214AC	Zener
	IC1	TLE6365	P-DSO-8	
	L1	220 µH	DX3316	Coilcraft power choke
	R1	2.2 kΩ	0805	
	R2	47 kΩ	0805	Switching frequency ~ 95 kHz
Input filter	C100	4.7 µF	7243	low ESR, e.g. EPCOS SpeedPower
	L100	15 µH	1812	EPCOS B82432-T1163-K
Output filter	L200	2.2 µH	1812	EPCOS B82432-T1222-K
	C200	47 nF	0805	X7R
	C201	47 nF	7243	low ESR, e.g. EPCOS SpeedPower

1) With output filter equipped
2) With output filter not equipped

4.2 EMC Filter Layout Recommendations

Figure 6 shows a section enlargement of the application PCB with input filter and output filter. The GND layer is an area located below the entire circuit. When this GND area is linked, no ground loops with other parts of the circuit on the board must be created.

Further layout recommendations (**Table 4**):

Table 4 Layout Recommendations 10-12

Number	Recommendation
10	Electrical shielding of choke L1. This can be done by placing a shielding winding or a case connected to GND made of a highly conductive material round the choke. Other possibilities include using a GND layer as large as possible. These measures minimize overall emission.
11	As highlighted in **Figure 6**, the distance between choke L1 and filter chokes L100 and L200 should be at least 20 mm to prevent disturbing coupling of the choke and filter chokes. This does not apply if L1 is fitted with a shielding case.
12	The GND terminals of filter capacitors C100, C200 and C201 should be directly connected to the GND shielding area.

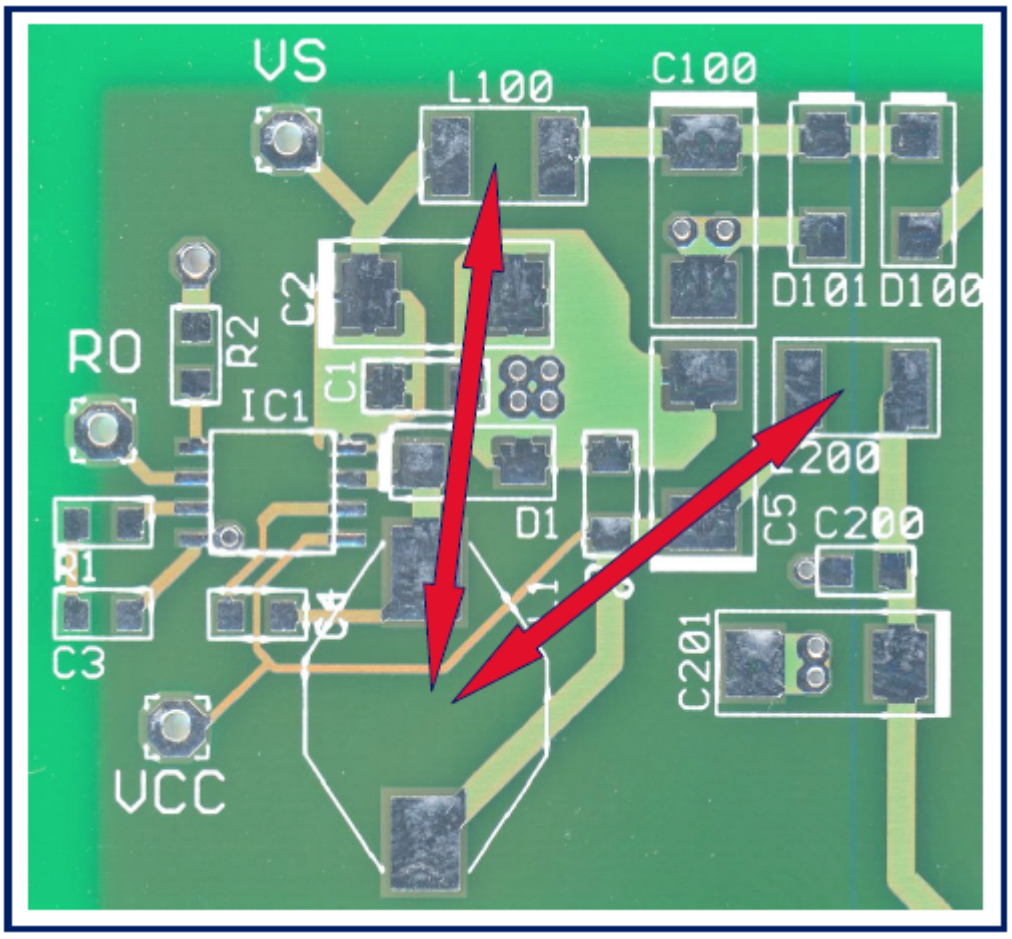

Figure 6 TLE6365 Application PCB with EMC Filters

5 Layout of the Application Circuit with Filtering

The ended application layout for the TLE6365 with additional EMC filter option is shown as a component placement drawing in **Figure 7**, as an equipped board in **Figure 8** and as top and bottom layer in **Figure 9** and **Figure 10**.

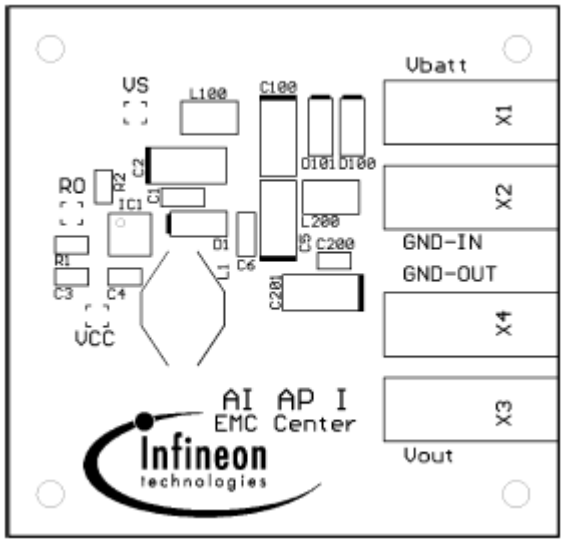

Figure 7 PCB Component Positions

Figure 8 Application Board

Layout of the Application Circuit with Filtering

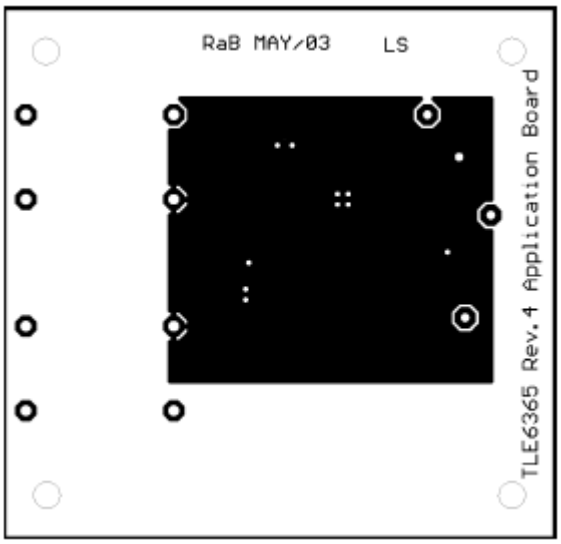

Figure 9 Bottom Layer of PCB

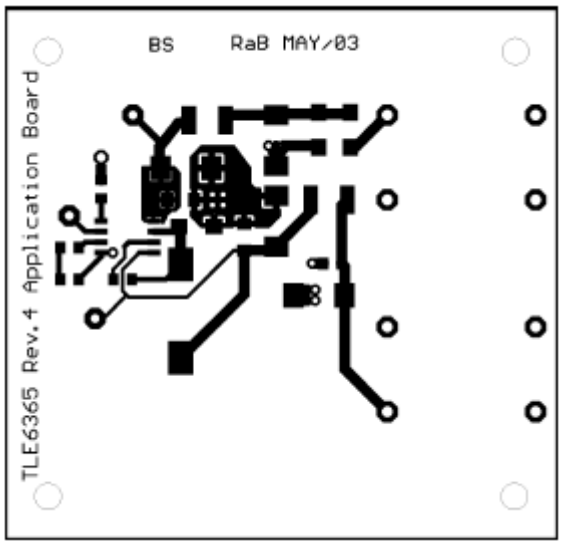

Figure 10 Top Layer of PCB

The size of the PCB is 66 mm x 64 mm.

6 EMC Results for TLE6365

6.1 Emission

6.1.1 Emission - Test Setup and Conditions

The emission of the TLE6365 application circuit was determined with the aid of the artificial network measurement according to CISPR 25. The device under test (DUT) is connected as shown in **Figure 11** via an artificial network (AN) simulating the typical impedance of an electrical vehicle power net. The high-frequency voltage on the artificial network was acquired by an EMI test receiver in peak detection mode.

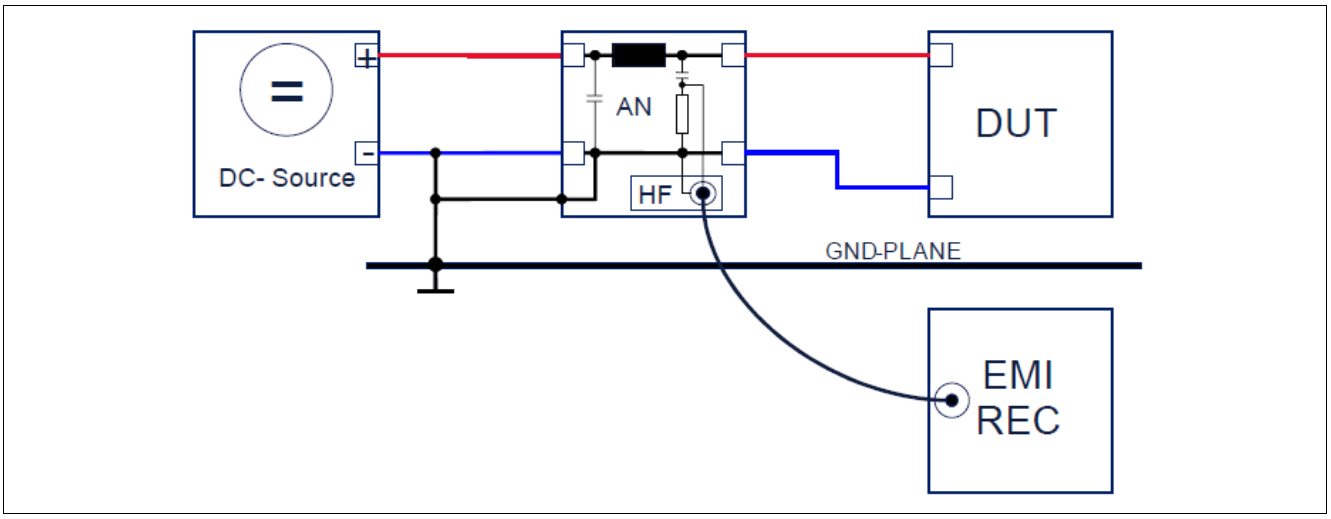

Figure 11 Scheme of the Conducted Emission Measurement

The test circuit was operated with different supply voltages, under different load conditions and with different filter connections as follows:

DUT: TLE6365 DateCode: 0109

Input voltage: 13.5 V / 27 V

Load resistance: 8.2 Ω / without load

Filtering: with / without

6.1.2 Emission - Measurement Results

The following diagrams show the measured emission for the application circuit operating under normal load and open-circuit conditions and the Class 1-5 limits for narrow-band disturbance according to CISPR 25. Each diagram also contains a noise curve showing the ambient conditions during measuring.

For applications on the 12 V vehicle electrical distribution system (V_s = 13.5 V), **Figure 12** shows the emission results on the supply line (V_s) from the application circuit with an optimized layout when no additional filter components are used. Depending on frequency range, results between EMI suppression class 1 and 3 can be achieved.

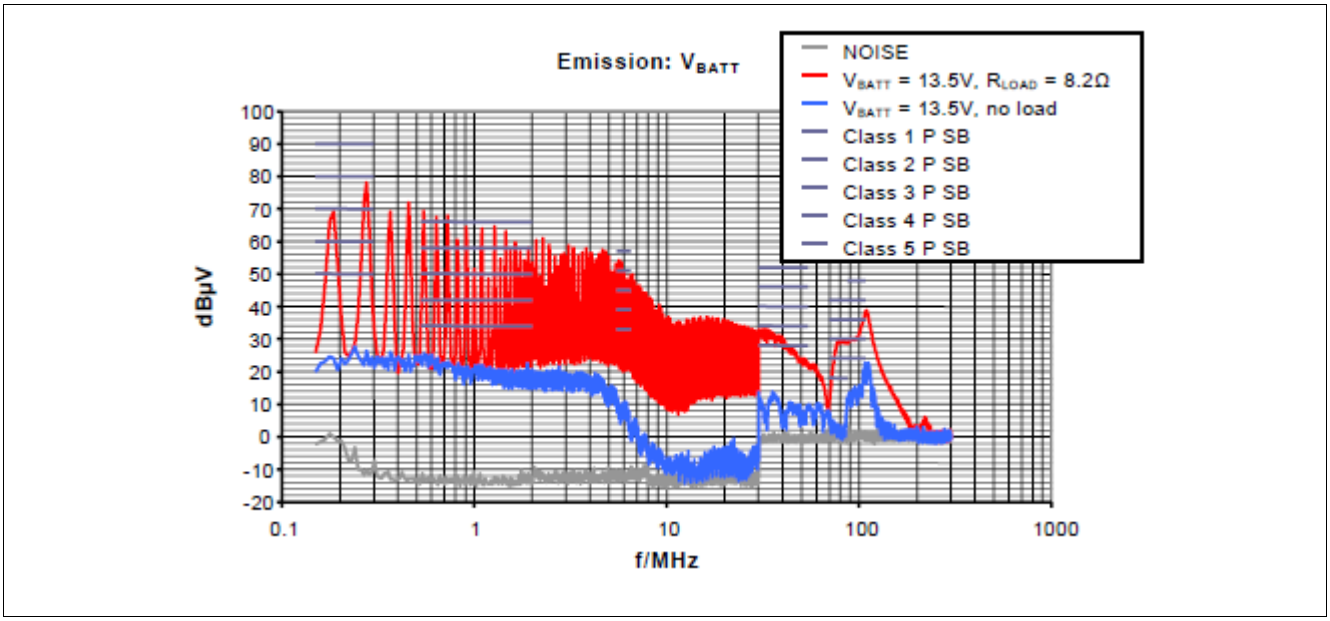

Figure 12 V_{BATT} Emission without Filter, V_{BATT} = 13.5 V

Figure 13 shows the emission results on the output voltage side (V_{OUT}) without any filter measures. In this case the values comply with EMI suppression class 3 to 5, depending on the frequency range.

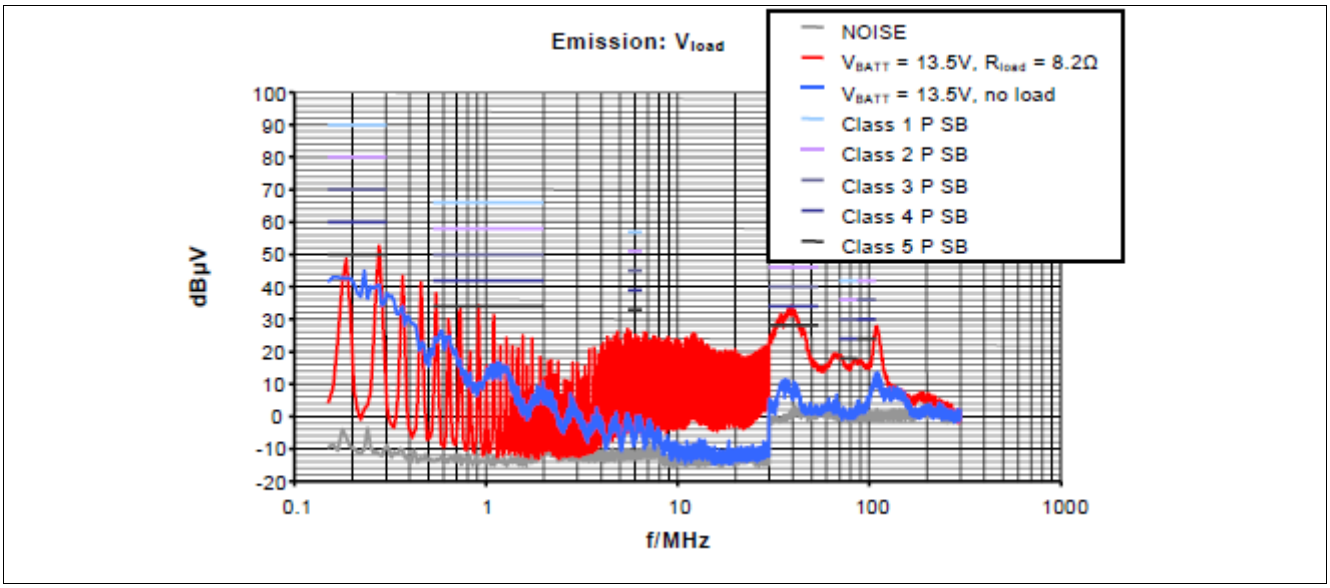

Figure 13 V_{Load} Emission without Filter, V_{BATT} = 13.5 V

If, in order to ensure compliance with EMI suppression class 5, the proposed filter components on the input side (L100=15 µH, C100=4.7 µF) and output side (L200=2.2 µH, C201=47 µF) are mounted in accordance with the layout recommendation, the measurement results are as follows. **Figure 14** shows the emission result for the input side (V_S) and **Figure 15** the emission result for the output side (V_{OUT}). The results were determined in each case with an input and output filter. However, they scarcely differ from the measurement results when only one filter is used. This means no mutual influencing between the filters could be established. For this reason the individual measurements are not shown.

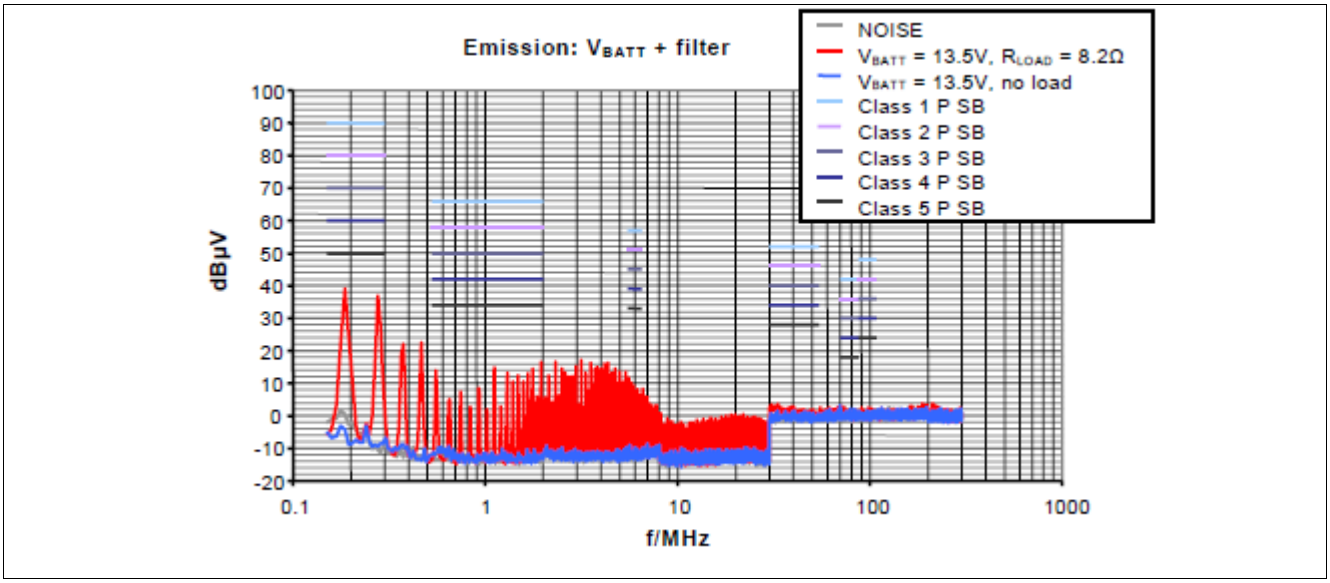

Figure 14 V_{BATT} Emission with Filter, V_{BATT} = 13.5 V

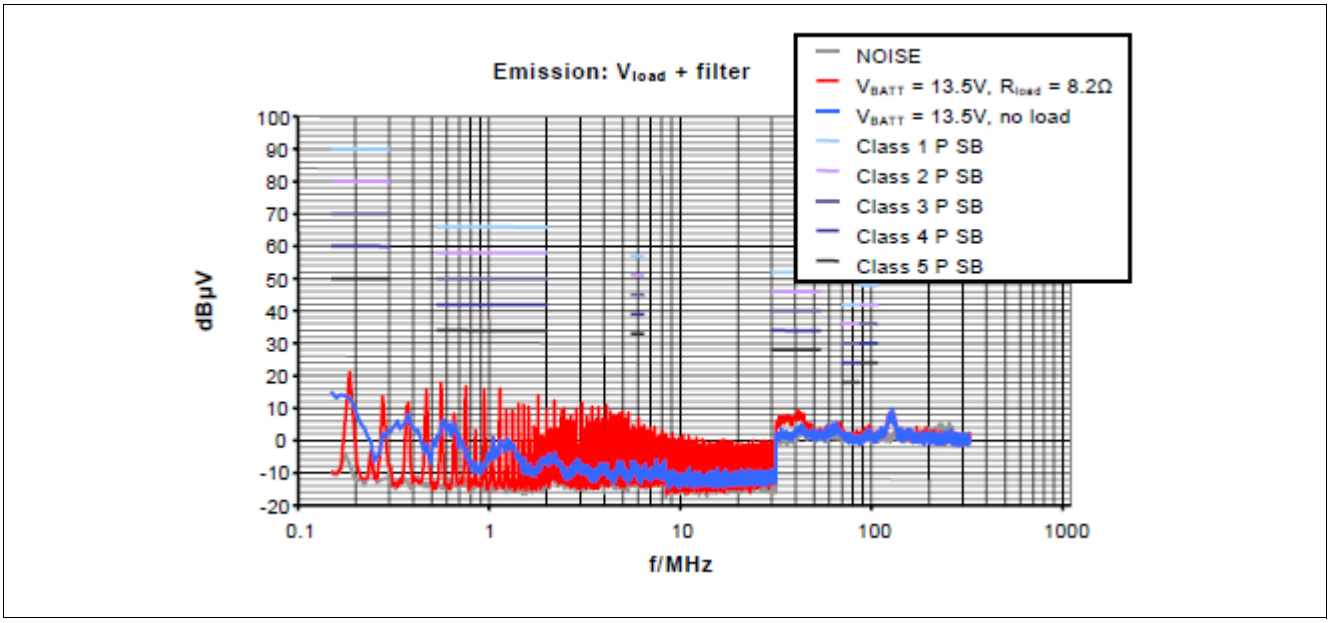

Figure 15 V_{Load} Emission with Filter, V_{BATT} = 13.5 V

The emission of the DC-DC converter application with the TLE6365 chip can be reduced by more than 10 dB below the most stringent limits of CISPR 25 Class 5 with the recommended filter components and layout guidelines. The results are similar for applications on the 24 V vehicle power net. **Figure 16** shows the emission results for the application circuit with an optimized layout and without a filter, measured on the supply line (V_S) with a supply voltage of 27 V. Results between EMI suppression classes 1 and 3 can be achieved depending on the frequency range.

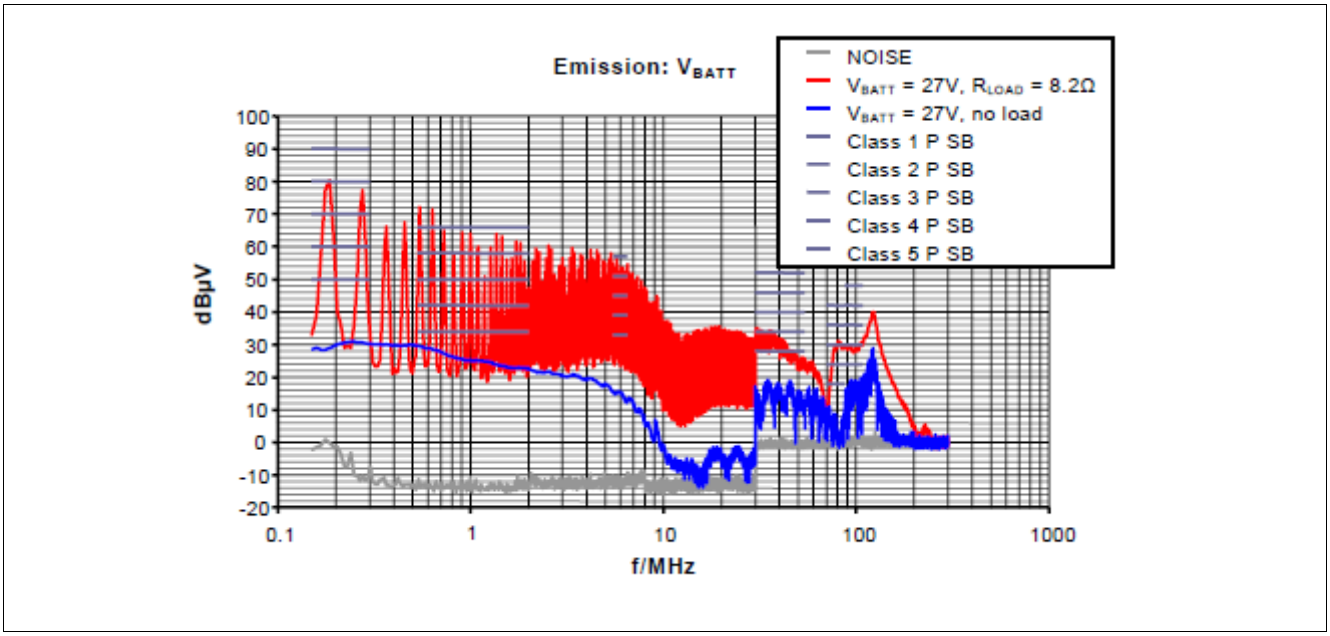

Figure 16 V_{BATT} Emission without Filter, V_{BATT} = 27 V

Figure 17 shows the emission results on the output voltage (V_{OUT}) at 27 V input voltage without any filter measures. In this case the values comply with EMI suppression classes 3 to 5, depending on the frequency range.

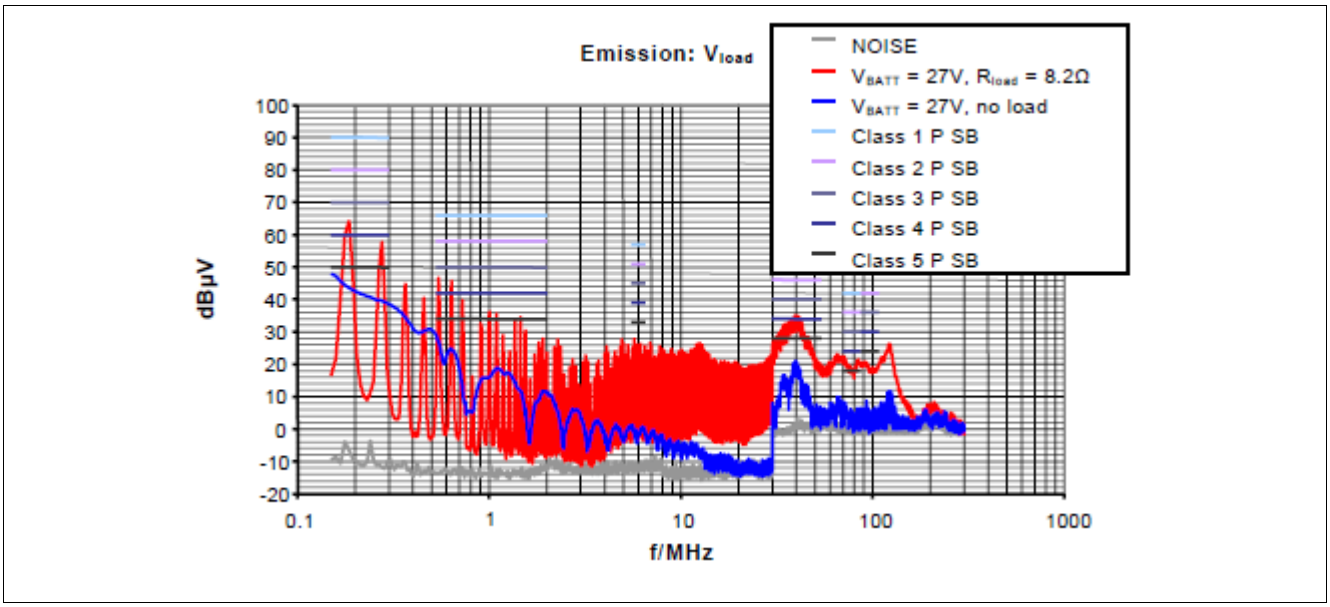

Figure 17 V_{Load} Emission without Filter, V_{BATT} = 27 V

With the filter components on the input side (L100=15 µH, C100=4.7 µF) and output side (L200=2.2 µH, C201=47 µF), the measurement results are as follows. **Figure 18** shows the emission result of the input side (V_s) and **Figure 19** the emission result of the output side (V_{OUT}) at an input voltage of 27 V. In this case, too, the results shown were determined using both input filter and output filter.

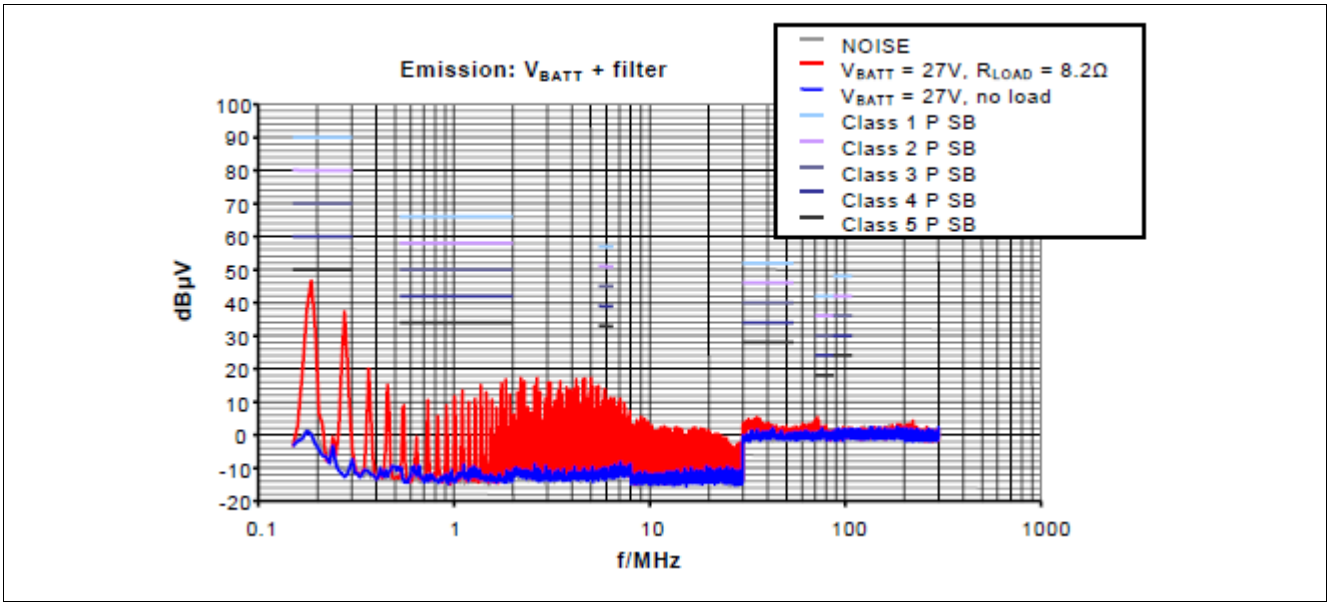

Figure 18 V_{BATT} Emission with Filter, V_{BATT} = 27 V

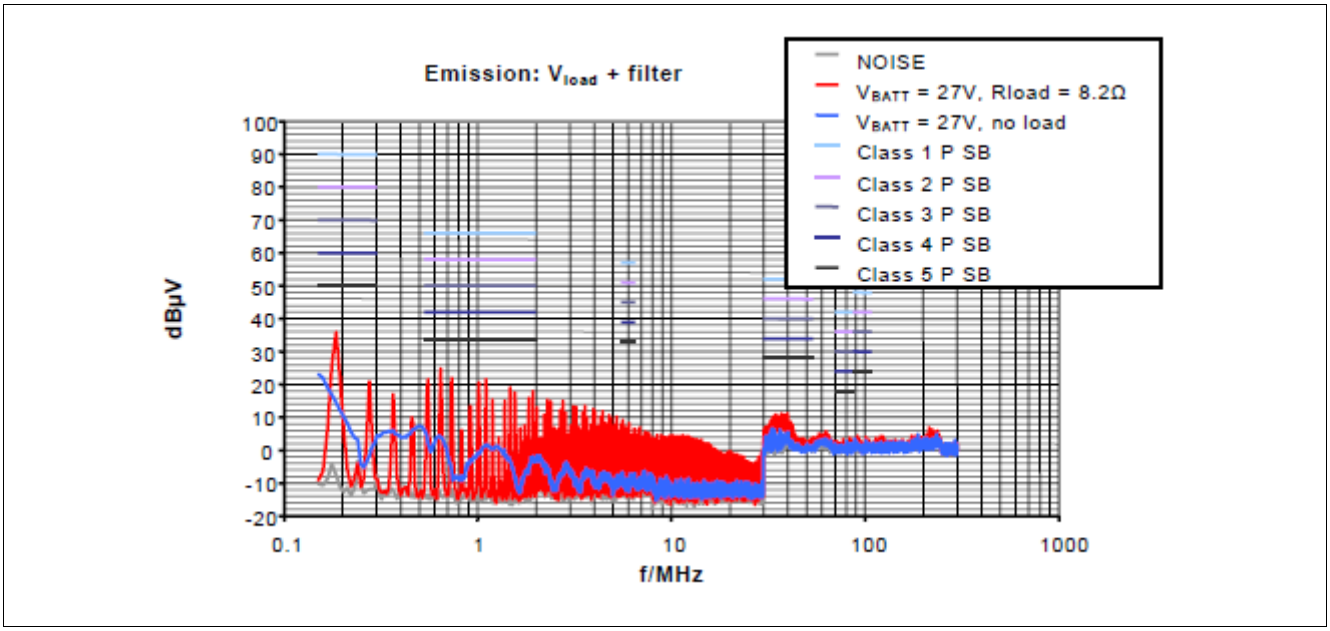

Figure 19 V_{Load} Emission without Filter, V_{BATT} = 27 V

With the same filter components recommended and the layout guidelines the emission of the DC-DC converter application with the TLE6365 chip can be reduced below the most stringent limits of CISPR 25 Class 5 even at higher supply voltage, like in the 24 V vehicle electrical power net. With the filter equipment recommended the application thus meets EMC requirements for a wide input voltage range.

6.2 RF Interference Immunity

6.2.1 RF Interference Immunity – Test Setup and Conditions

The RF interference immunity of the TLE6365 was tested using the Direct Power Injection Method (DPI) according to IEC62132-4. With this method, RF power is coupled onto a terminal or pin being tested on a selected frequency basis in a frequency range from 150 kHz to 1 GHz, and a check is carried out to determine whether the application operates within the specified limits or at what power level and frequency the specifications are not met. **Figure 20** shows the basic measurement setup. The high-frequency signal set by the control PC is amplified and coupled onto the IC or circuit. The IC's operation is monitored, e.g. with an oscilloscope. Any malfunction is reported to the control PC. The system determines and logs the maximum RF power that can be applied for each frequency. The result is a chart that shows the limit rating across the frequency range at which the application operates within the specified ratings.

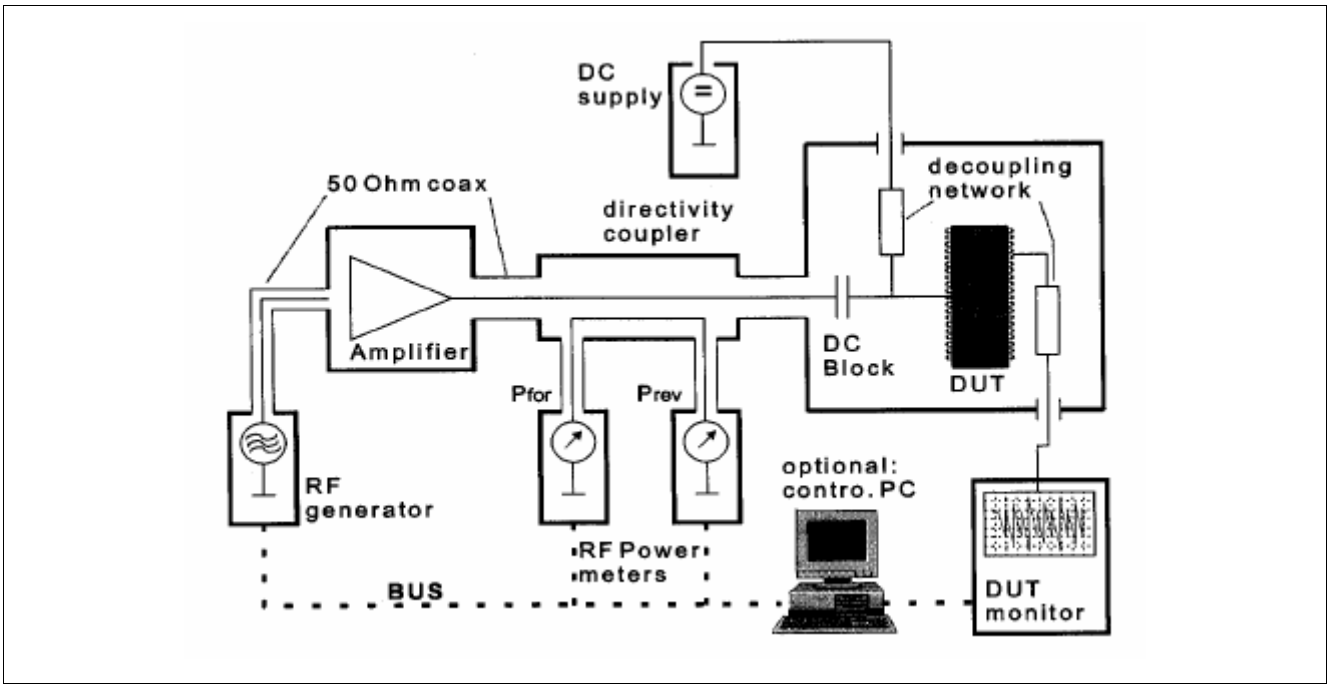

Figure 20 Outline of DPI Test Setup

The test circuit is operated at different supply voltage and in different load conditions for the RF interference immunity tests as follows. The filter circuit developed to ensure compliance with the emission limits is employed as standard for these tests.

DUT: TLE6365 DateCode: 0109

Input voltage: 13. 5V / 27 V

Load resistance: 8.2 Ω / without load

Filtering: with

During measuring the output voltage V_{OUT} at 5 V +/-100 mV and the reset voltage V_{RO}=5V +/- 0.4V were monitored as a fault criterion for the application operating in accordance with the specifications. Power was coupled onto the supply voltage (V_{BATT}) and the output voltage (V_{OUT}).

6.2.2 RF Interference Immunity – Measurement Results

The interference immunity diagrams show the self-specified power limit of 37 dBm (5 W) and the power curves of the TLE6365 application that were determined. **Figure 21** shows the application's interference immunity characteristics when RF power is coupled onto the supply line with 13.5 V and 27 V supply voltage with and

without output loading. Except at 650 MHz, the result corresponds to the self-specified limit. The power drop of 3...5 dB is due to resonance on the PCB at which the attenuation of the filters is too low. Output voltage drops in the event of a fault. This is detected by the built in monitoring of the chip and indicated at RO.

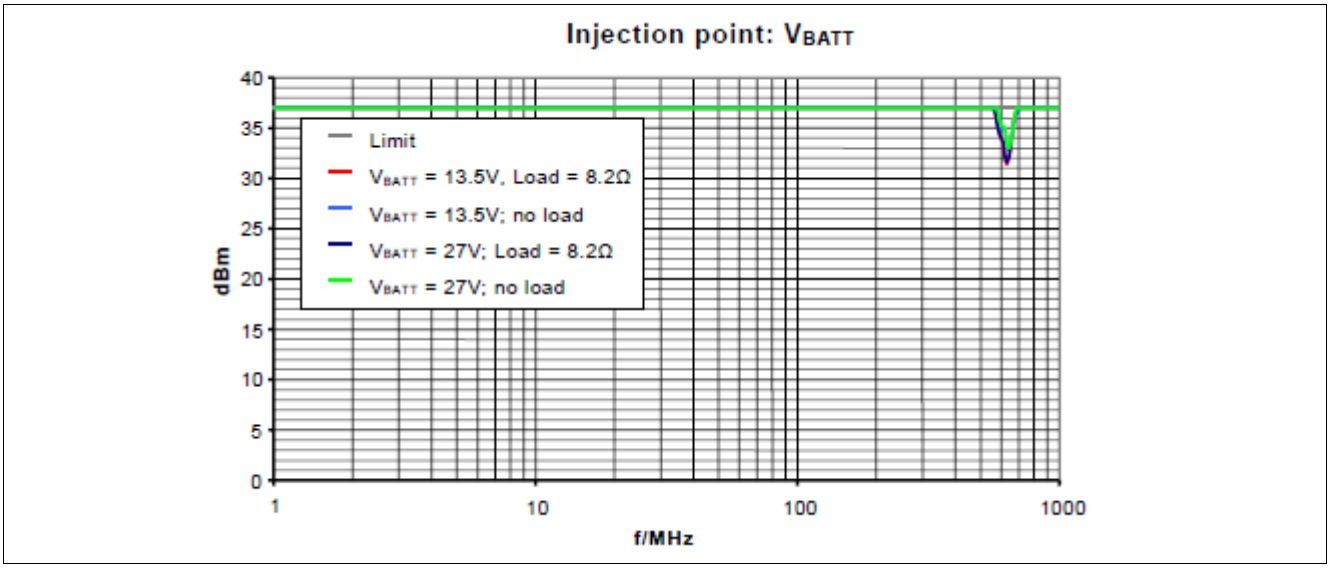

Figure 21 DPI Results: V_{BATT}

For comparison, **Figure 22** shows the result when power is coupled onto the output (V_{OUT}) at an input voltage of 27 V. Interference immunity drops by up to 2 dB in the frequency range around 600 MHz, similarly to when power is coupled onto the input. The result is only shown for input voltage of 27 V as no dependency for the interference immunity from input voltage was established. The application test circuit achieves a very high immunity to RF interference with these values.

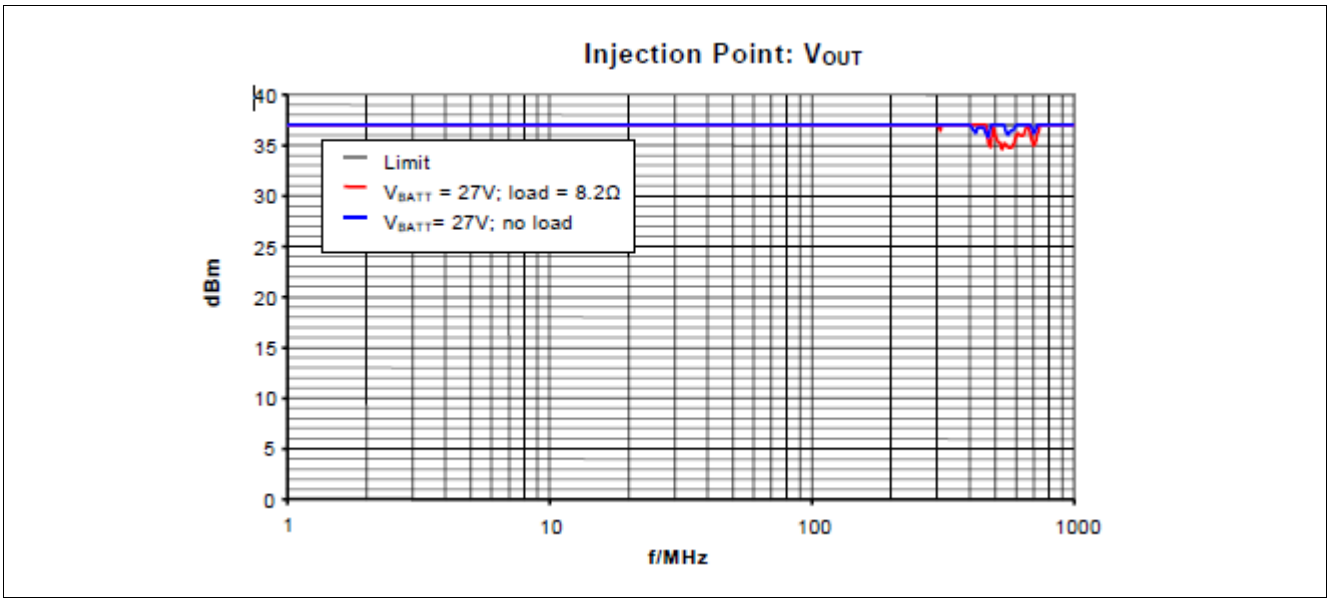

Figure 22 DPI Results: V_{Out}

6.3 Pulse Interference Immunity

6.3.1 Pulse Interference Immunity – Test Setup and Conditions

Pulses are generated during switching cycles in an automobile's electrical power net which superimpose the supply voltage V_{BATT}. These pulses are described in ISO 7637. The circuit's response to the pulses is classified in five categories as shown in **Table 5**:

Table 5 Function Classes of Pulse Response

Class	Value
A	All functions of a device/system perform as designed during and after exposure to disturbance
B	All functions of a device/system perform as designed during exposure. However, one or more of them can exceed the specified tolerance. All functions return automatically to within normal limits after exposure is removed. Memory functions shall remain class A
C	One or more functions do not perform as designed during exposure but return automatically to normal operation after exposure is removed
D	One or more functions of a device/system do not perform as designed during exposure and do not return to normal operation until exposure is removed and the device/ system is reset by simple "operator/user" action
E	One or more functions of a device/system do not perform as designed during and after exposure and cannot be returned to proper operation without repairing or replacing the device/system

During pulse interference immunity tests, a test pulse generator injects these positive and negative disturbance voltage pulses onto the supply voltage to which the application circuit is connected.

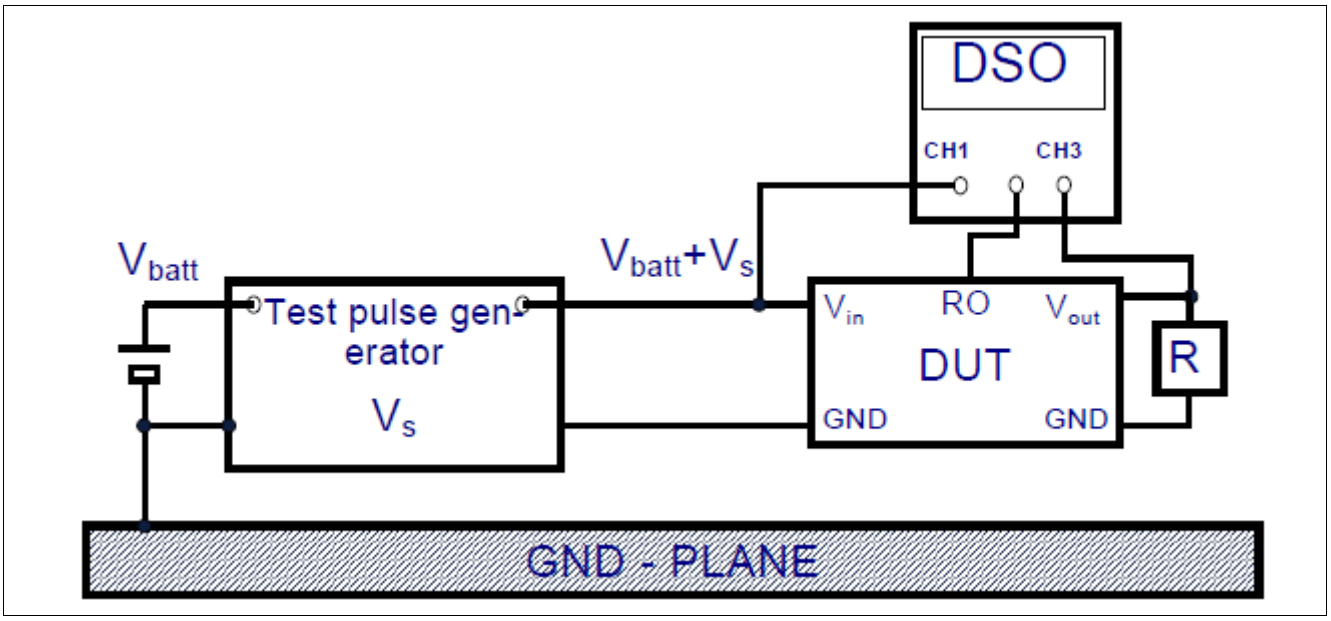

Figure 23 Test Setup: Pulse Interference Immunity

The pulse interference immunity tests were carried out using a supply voltage of 13.5 V with load and filter:
DUT: TLE6365 DateCode: 0109
Input voltage: 13.5 V

Load resistance: 8.2 Ω

Filtering: with

To monitor operation in accordance with the specifications, the output voltage V_{OUT} at 5 V +/- 100 mV and reset voltage V_{RO} = 5 V +/- 0.4 V were measured using an oscilloscope.

6.3.2 Pulse Interference Immunity – Measurement Results

Table 6 shows the functional status classes achieved by the test application for the types of test pulses tested and the respective test voltage levels.

Table 6 Test Results: ISO 7637 (Fast Electrical Transients)

Test Pulse	Max. Test Level V_S	Test Results with R_{Load} = 8.2 Ω	Pulse Cycle Time and Generator Impedance	Monitoring
1	-200 V	C[1)]	500 ms; 10 Ω	V_{batt} V_{out} RO
2	+200 V	C[1)]	500 ms; 10 Ω	
3a	-200 V	C[2)]	500 ms; 50 Ω	
3b	+200 V	C[2)]	500 ms; 50 Ω	
4	-7 V	C[3)]	0.01 Ω	
5[4)]	–	–	–	

1) Supply voltage is interrupted for 200 ms for pulses 1 and 2. The 22 µF input capacitor is unable to bypass this time with a load of 3 W. As a result, output voltage drops until the supply voltage is reapplied. This results in function class C.

2) With the fast pulses 3a and 3b the pulse peaks couple onto the output and, depending on the monitoring method, are detected. If these peaks are rated, the output voltage is outside the specifications. If the mean voltage is rated or if sampling is slower, function class A would be reached.

3) With pulse 4 the capacitance of the input capacitor is not sufficient to supply the power needed to bypass under-voltage time. This results in function class C.

4) Measuring the load dump interference immunity with pulse 5 according to ISO 7637 was dispensed with because, on one hand, central load dump protection is becoming increasingly established and, on the other hand, the power content of pulse 5 would have to be carried by the polarity protection and Zener diode or a suppressor diode.

7 Summary

The circuit design and layout measures for an application circuit show that automotive EMC requirements can be met through selective design measures. Optimized layout is essential, but not sufficient for meeting EMC requirements. The most stringent Class 5 emission limits of CISPR 25 can be met by incorporating two filter components in the layout of the application circuit in an optimized way. The circuit proposed here is dimensioned in a way that the application meets EMC requirements over a wide range of input voltage. The results shown for emission, RF and pulse interference immunity can be achieved with the design proposed.

8 Revision History

Revision	Date	Changes
1.01	2015-04-23	Infineon Style Guide update. Editorial changes.
1.0	2003-11-01	Application Note created.

Trademarks of Infineon Technologies AG

AURIX™, C166™, CanPAK™, CIPOS™, CIPURSE™, CoolGaN™, CoolMOS™, CoolSET™, CoolSiC™, CORECONTROL™, CROSSAVE™, DAVE™, DI-POL™, DrBLADE™, EasyPIM™, EconoBRIDGE™, EconoDUAL™, EconoPACK™, EconoPIM™, EiceDRIVER™, eupec™, FCOS™, HITFET™, HybridPACK™, ISOFACE™, IsoPACK™, i-Wafer™, MIPAQ™, ModSTACK™, my-d™, NovalithIC™, OmniTune™, OPTIGA™, OptiMOS™, ORIGA™, POWERCODE™, PRIMARION™, PrimePACK™, PrimeSTACK™, PROFET™, PRO-SIL™, RASIC™, REAL3™, ReverSave™, SatRIC™, SIEGET™, SIPMOS™, SmartLEWIS™, SOLID FLASH™, SPOC™, TEMPFET™, thinQ!™, TRENCHSTOP™, TriCore™.

Other Trademarks

Advance Design System™ (ADS) of Agilent Technologies, AMBA™, ARM™, MULTI-ICE™, KEIL™, PRIMECELL™, REALVIEW™, THUMB™, µVision™ of ARM Limited, UK. ANSI™ of American National Standards Institute. AUTOSAR™ of AUTOSAR development partnership. Bluetooth™ of Bluetooth SIG Inc. CAT-iq™ of DECT Forum. COLOSSUS™, FirstGPS™ of Trimble Navigation Ltd. EMV™ of EMVCo, LLC (Visa Holdings Inc.). EPCOS™ of Epcos AG. FLEXGO™ of Microsoft Corporation. HYPERTERMINAL™ of Hilgraeve Incorporated. MCS™ of Intel Corp. IEC™ of Commission Electrotechnique Internationale. IrDA™ of Infrared Data Association Corporation. ISO™ of INTERNATIONAL ORGANIZATION FOR STANDARDIZATION. MATLAB™ of MathWorks, Inc. MAXIM™ of Maxim Integrated Products, Inc. MICROTEC™, NUCLEUS™ of Mentor Graphics Corporation. MIPI™ of MIPI Alliance, Inc. MIPS™ of MIPS Technologies, Inc., USA. muRata™ of MURATA MANUFACTURING CO., MICROWAVE OFFICE™ (MWO) of Applied Wave Research Inc., OmniVision™ of OmniVision Technologies, Inc. Openwave™ of Openwave Systems Inc. RED HAT™ of Red Hat, Inc. RFMD™ of RF Micro Devices, Inc. SIRIUS™ of Sirius Satellite Radio Inc. SOLARIS™ of Sun Microsystems, Inc. SPANSION™ of Spansion LLC Ltd. Symbian™ of Symbian Software Limited. TAIYO YUDEN™ of Taiyo Yuden Co. TEAKLITE™ of CEVA, Inc. TEKTRONIX™ of Tektronix Inc. TOKO™ of TOKO KABUSHIKI KAISHA TA. UNIX™ of X/Open Company Limited. VERILOG™, PALLADIUM™ of Cadence Design Systems, Inc. VLYNQ™ of Texas Instruments Incorporated. VXWORKS™, WIND RIVER™ of WIND RIVER SYSTEMS, INC. ZETEX™ of Diodes Zetex Limited.

Trademarks Update 2014-07-17

www.infineon.com

Edition 2015-04-23

Published by

Infineon Technologies AG

81726 Munich, Germany

© 2014 Infineon Technologies AG.

All Rights Reserved.

Do you have a question about any aspect of this document?

Email: erratum@infineon.com

Document reference
Doc_Number

Legal Disclaimer

THE INFORMATION GIVEN IN THIS APPLICATION NOTE (INCLUDING BUT NOT LIMITED TO CONTENTS OF REFERENCED WEBSITES) IS GIVEN AS A HINT FOR THE IMPLEMENTATION OF THE INFINEON TECHNOLOGIES COMPONENT ONLY AND SHALL NOT BE REGARDED AS ANY DESCRIPTION OR WARRANTY OF A CERTAIN FUNCTIONALITY, CONDITION OR QUALITY OF THE INFINEON TECHNOLOGIES COMPONENT. THE RECIPIENT OF THIS APPLICATION NOTE MUST VERIFY ANY FUNCTION DESCRIBED HEREIN IN THE REAL APPLICATION. INFINEON TECHNOLOGIES HEREBY DISCLAIMS ANY AND ALL WARRANTIES AND LIABILITIES OF ANY KIND (INCLUDING WITHOUT LIMITATION WARRANTIES OF NON-INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS OF ANY THIRD PARTY) WITH RESPECT TO ANY AND ALL INFORMATION GIVEN IN THIS APPLICATION NOTE.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office. Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.