

Robust Dimensioning of the Output Capacitor

TLE727x-2 – Ultra-Low Quiescent Current LDOs

Z8F52274290

Application Note

Rev. 1.01, 2014-09-26

Automotive Power

Table of Contents

1	Abstract	3
2	Introduction	4
3	Theoretical Background on Ultra-Low Quiescent Current Control Loop Concepts	5
3.1	Influence of Control Loop's Reaction Time on Output Voltage	5
3.2	Influences on Control Loop's Reaction Time	8
3.3	Consequences for the Application	10
3.4	Influence of the Output Capacitor	12
3.5	Conclusion	14
4	Dimensioning the Output Capacitor of an Ultra-Low Quiescent Current Voltage Regulator	15
4.1	How to Avoid Big Current Transients	15
4.2	How to Dimension the Output Capacitor	15
5	Additional Information	23
6	Revision History	24

Abstract

1 Abstract

Note: The following information is given as a hint for the implementation of our devices only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

This Application Note is intended to provide a description on how to dimension the output capacitor of a linear voltage regulator with ultra-low quiescent current to obtain a reliable supply circuit.

Introduction

2 Introduction

In nearly all of today's electronic systems, low energy consumption is one of the major challenges. As the systems' performance is increasing in all kinds of applications, intelligent solutions need to be found to compensate at the same time the increasing energy demand. These then help either to save energy costs or to efficiently use limited energy resources.

One example for limited energy resources can be found within the automotive area: The car's battery provides a limited amount of energy. Therefore, any electronic system being permanently connected to the battery faces hard requirements regarding its energy consumption.

For supply ICs, saving energy means keeping the internal current consumption as low as possible. The challenge is here to ensure a proper operation at very low bias currents of all functionalities that are usually present within the IC.

To meet these requirements for linear voltage regulators, Infineon has set a benchmark on the market with its ultra-low quiescent current voltage regulators. These products combine, besides the usual functionalities and an outstanding quality, sophisticated feature sets like Window-Watchdog and Reset with an ultra-low current consumption of only 28 μ A (TLE7273-2). Without additional features, the ultra-low quiescent current voltage regulators reach a current consumption of even 20 μ A (TLE7274-2). In addition, to reduce the overall system cost, Infineon implemented for these regulators an advanced control loop concept that requires only a very small output capacitor for control loop stability.

This document is split in two parts: In the first one ([Chapter 3](#)), the challenge for circuit design for linear voltage regulators of combining ultra-low quiescent current with very small output capacitors is demonstrated. The second part ([Chapter 4](#)) shows a procedure for dimensioning the output capacitor to set up a reliable and robust supply circuit with ultra-low quiescent current. Therefore, if you're just interested in quickly setting up your application using an ultra-low quiescent current linear voltage regulator, you can skip the theoretical part and directly jump to [Chapter 4](#).

3 Theoretical Background on Ultra-Low Quiescent Current Control Loop Concepts

In this chapter, the challenge for circuit design of combining in a linear voltage regulator ultra-low quiescent current with very small output capacitors is demonstrated.

For this, we'll look inside a linear voltage regulator and have a closer look on the influence of the output capacitor.

3.1 Influence of Control Loop's Reaction Time on Output Voltage

The main part of every linear voltage regulator is the integrated control loop, that is controlling the voltage regulator's output voltage. Depending on the application requirements, different control loop concepts can be implemented. Each one of these has different advantages and disadvantages regarding their performance. One important criterion for performance of a control loop is its so-called "reaction time". Let's see what it is and why it is important:

Figure 1 shows a simple application circuit with a microcontroller supplied by a linear voltage regulator. Let's assume that the application has a standby mode and a normal operating mode, but is never completely shut down. This means the microcontroller is always supplied, but in standby mode with few mA or even less (let's take 1mA as simple example), in normal operating mode with several 10mA up to few 100mA (let's assume 70mA). Now, at the moment the microcontroller is triggered to go from standby mode to normal operating mode, the result is typically a fast current transient with rise times below 500ns at the voltage regulator's output.

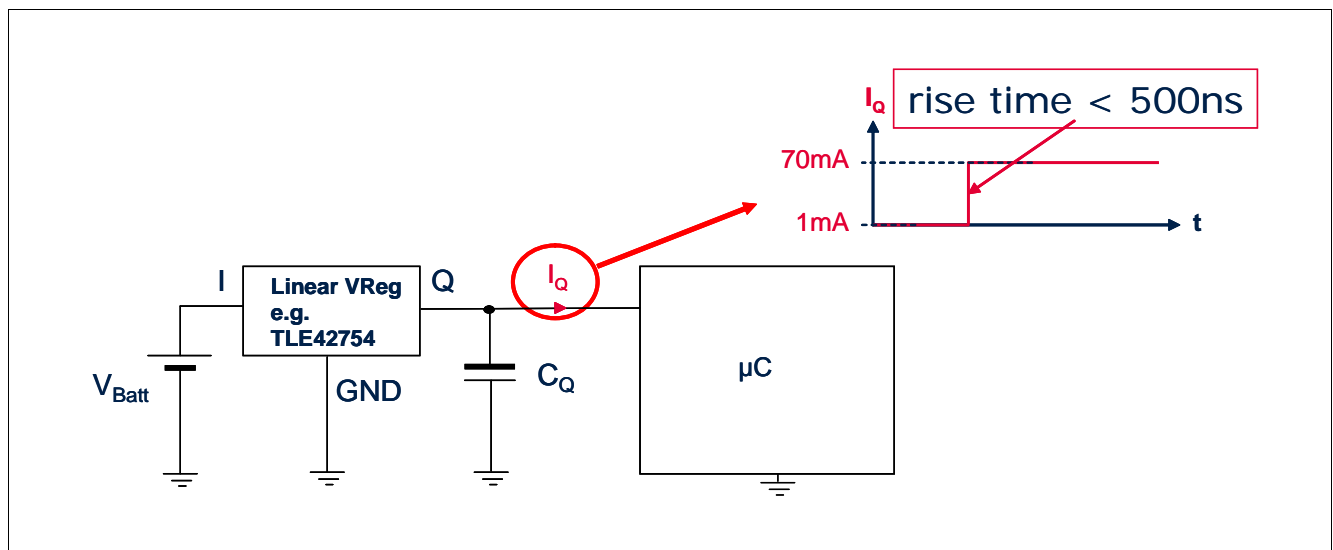


Figure 1 Simple Application Circuit

Figure 2 shows the typical behaviour of a standard (not ultra-low quiescent current) linear voltage regulator at this current transient. The output voltage is set to 5V. It can be seen that at the moment of the current transient, the voltage is dropping down by ΔV to a minimum value ("Min. Voltage"). During this phase, the voltage regulator's control loop is not reacting yet. Only after this short time, called "Reaction Time", the control loop is acting and sets the output voltage back to the nominal value by increasing the output current.

It is now obvious that the reaction time is a performance criterion for a control loop as: The faster the control loop's reaction time, the smaller the voltage drop at current transients.

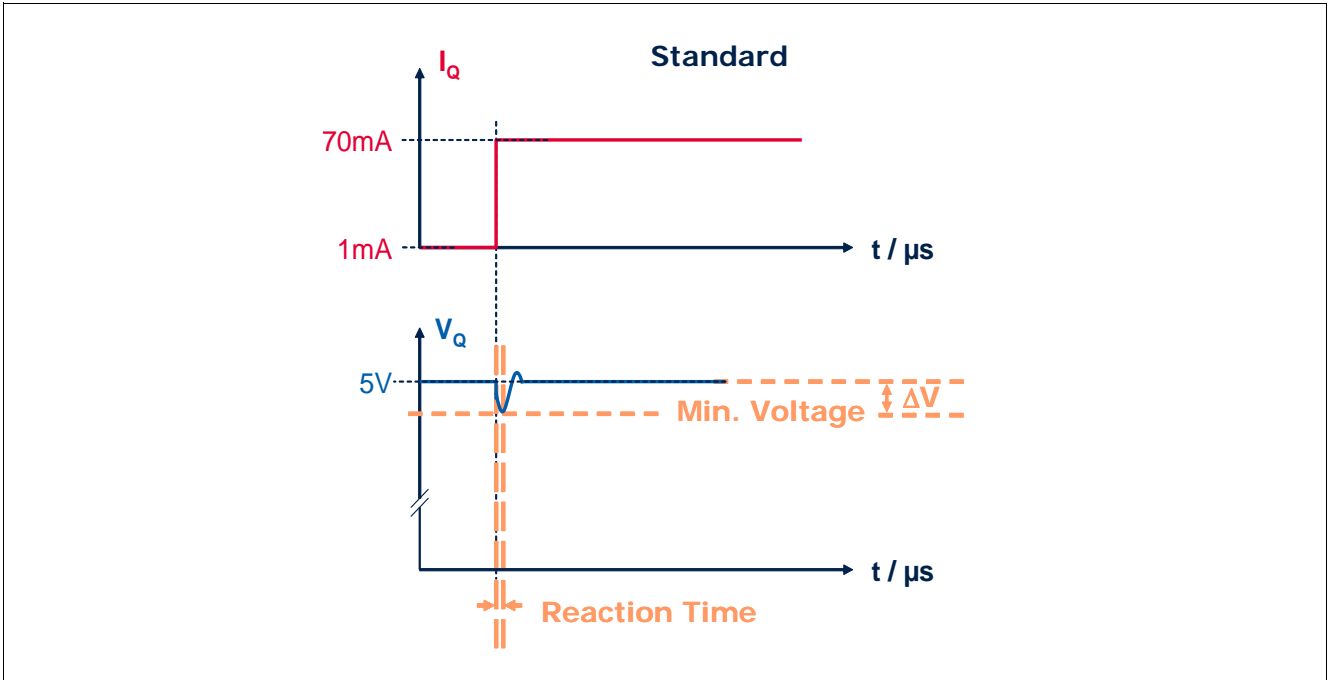


Figure 2 Output Voltage at Current Transient at Standard Linear Voltage Regulator

In case the microcontroller is triggered to go from normal operating mode to stand-by mode, a negative current transient is resulting and the behaviour is the other way round. This is shown in **Figure 3**. The correlation between ΔV and reaction time is the same, the faster the reaction time, the smaller the voltage peak.

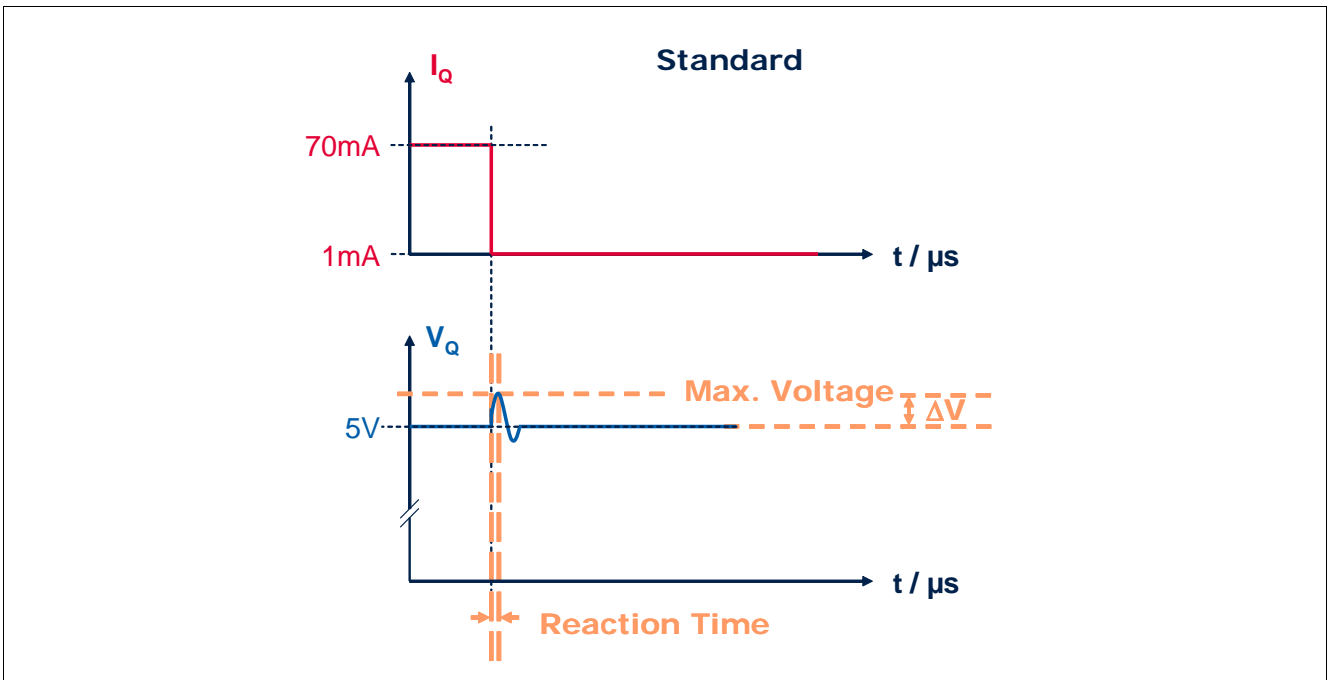


Figure 3 Output Voltage at Negative Current Transient at Standard Linear Voltage Regulator

Theoretical Background on Ultra-Low Quiescent Current Control Loop Concepts

Let's now focus on the reaction time of a control loop of an ultra-low quiescent current linear voltage regulator.

Figure 4 shows now in addition the output voltage of an ultra-low quiescent current linear voltage regulator (right picture). It can be easily seen that its reaction time is longer, hence its voltage drop higher.

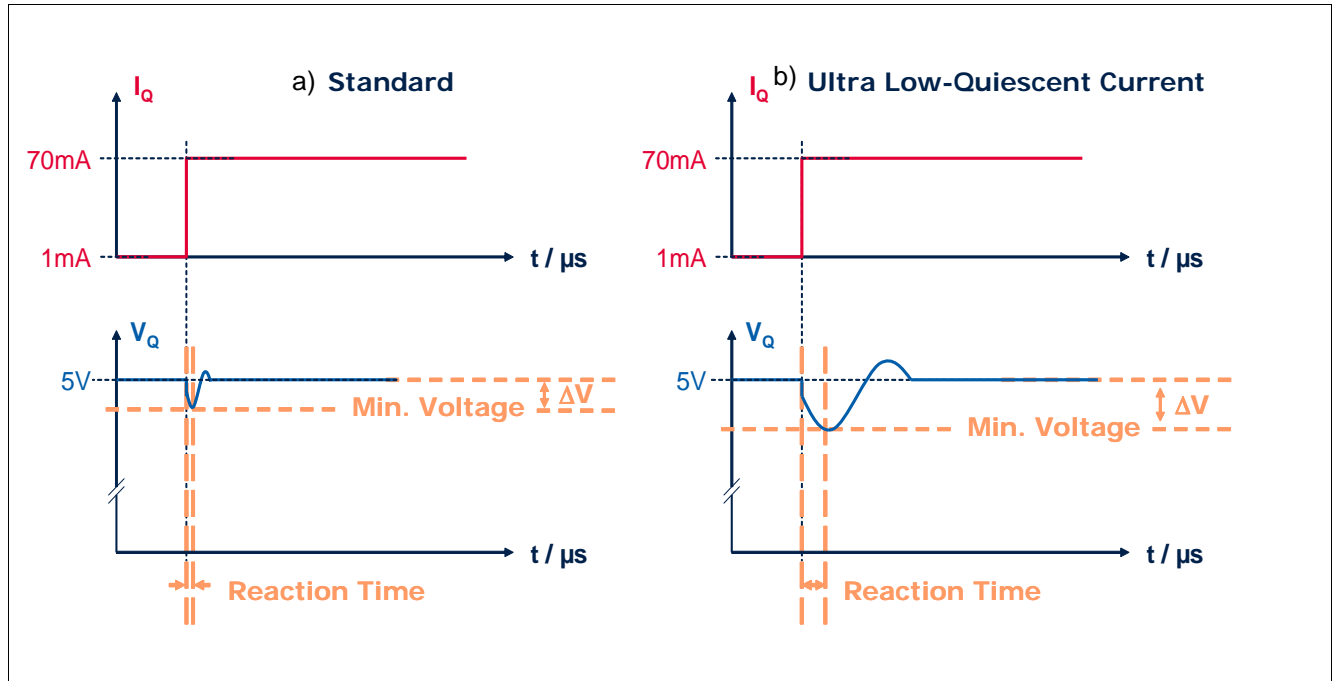


Figure 4 Output Voltage at Current Transient: a) Standard versus b) Ultra-low Quiescent Current Linear Voltage Regulator

The same conclusion can be found at a negative current transient shown in **Figure 5**: The control loop's reaction time at an ultra-low quiescent current voltage regulator is longer, therefore the voltage peak is higher.

Theoretical Background on Ultra-Low Quiescent Current Control Loop Concepts

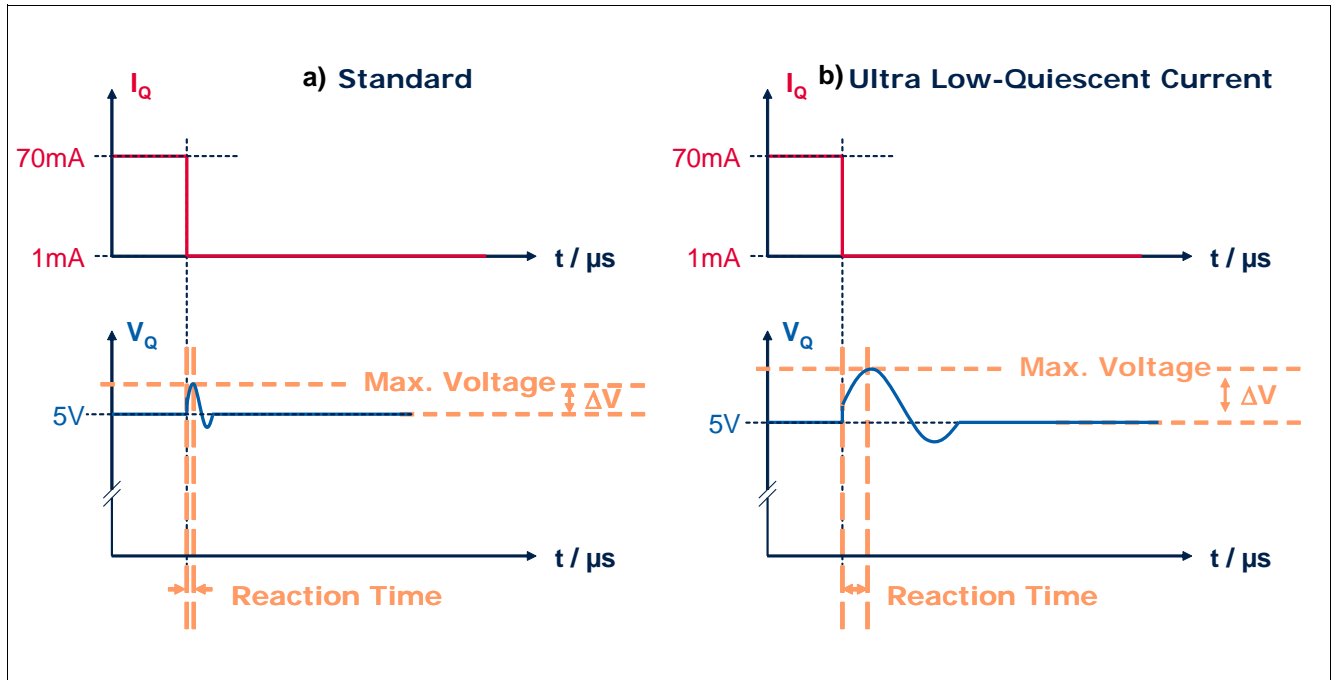


Figure 5 Output Voltage at Negative Current Transient: a) Standard versus b) Ultra-low Quiescent Current Linear Voltage Regulator

Thus the question is: Why is the reaction time of an ultra-low quiescent current linear voltage regulator higher than that for a standard one?

3.2 Influences on Control Loop’s Reaction Time

Therefore, let’s discuss the influences on the control loop’s reaction time.

For this, we’ll look inside a linear voltage regulator. **Figure 6** delivers a simplified insight, one can see that all basic functions like the voltage reference, the error amplifier and the protection functions need to be biased.

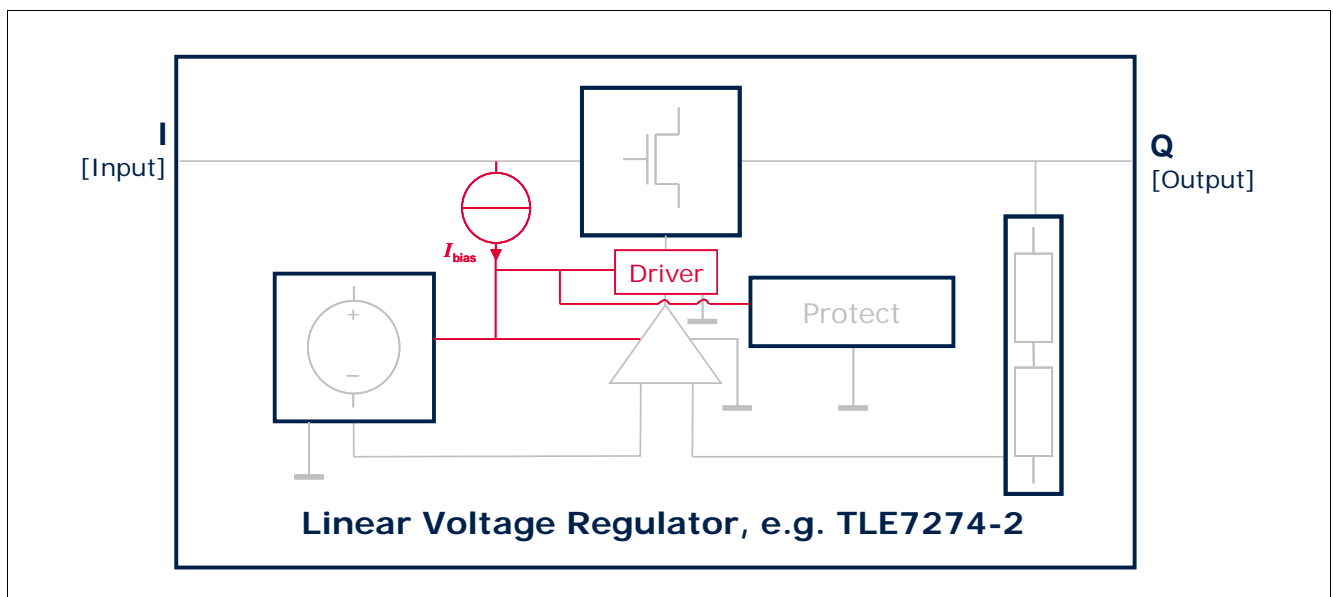


Figure 6 Biasing inside a Linear Voltage Regulator

Theoretical Background on Ultra-Low Quiescent Current Control Loop Concepts

But what has biasing to do with reaction time, where do the delays come from?

In silicon technology, delays are generally caused by capacitances. Let's now see, why these capacitances are present. Some of these are intentionally integrated capacitors, added by the IC designer, some of them are unwanted, but inevitable due to the used silicon technology. These are then the so-called parasitic capacitances.

Both types cause delays within the silicon according to [Equation \(3.1\)](#)

$$t_{\text{delay}} = \frac{C \cdot \Delta V}{I_{\text{bias}}} \quad (3.1)$$

Note: This simplified formula provides a sufficient indication as bias currents and capacitance values are nearly constant.

Let's now apply one theoretical example: Assume that the bias current for a device is $I_{\text{bias}} = 30 \mu\text{A}$, an integrated capacitor has $C = 30 \text{ pF}$, and there's a voltage delta of $\Delta V = 1 \text{ V}$. The calculated delay according to [Equation \(3.1\)](#) would be then $t_{\text{delay}} = 1 \mu\text{s}$.

Parasitic Capacitances

This type of capacitance is unwanted, but present in every silicon technology. It is typically not one specific capacitor, but a capacitance value that is resulting from several parasitic effects. Hence it is difficult to quantize it to concrete values, but we'll at least give an indication here: Depending on the silicon technology, it is normally in the range of several pF and has at linear voltage regulators a minor, but not neglectable influence on delays. By using the above formula and a voltage delta of $\Delta V = 0.5 \text{ V}$, one would get delays in the range of $0.5 \mu\text{s} \dots 1 \mu\text{s}$ per capacitance for an ultra-low quiescent current concept, for a non-ultra-low quiescent current concept considerably less ($t_{\text{delay}} < 0.05 \mu\text{s}$ per capacitor). Again, these values are intended as theoretical indication to understand the influence of parasitics within the technology on the delays, in real products different values can occur.

Power Stage

Depending on the application's requirements, different kinds of power stages are used for linear voltage regulators. Basically two types of power stage families can be found, bipolar types and MOSFET types.

To get an idea on the delays occurring in these different types, let's simplify their circuitry like shown in [Figure 7](#). Also here, all values need to be considered as indication to understand the power stage's influence on delays, as well as the difference between concepts and power stage types. Real products might show different values.

Theoretical Background on Ultra-Low Quiescent Current Control Loop Concepts

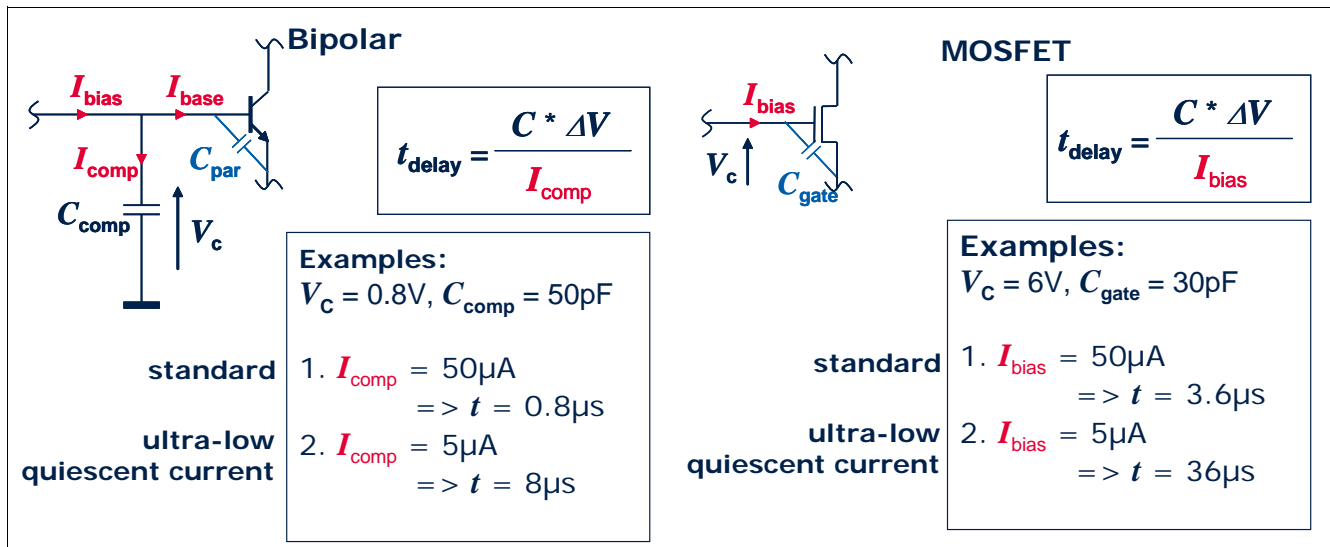


Figure 7 Delays in Power Stages

In a bipolar power stage, the main delay results from the compensation capacitor and the parasitic base capacitance. In a MOSFET power stage, the delay is caused by the gate capacitance, worst case occurs during start-up, when the gate capacitance needs to be fully charged ($\Delta V = V_C = 6\text{V}$).

Important to notice is that the delay caused by MOSFET power stages is typically higher, and the delay caused by ultra-low quiescent current concepts is even higher.

To sum up, the longest delay is caused by the combination of an ultra-low quiescent current concept with a MOSFET power stage. Therefore, linear voltage regulators implementing this combination show a slower reaction time of the control loop than standard linear voltage regulators.

Output Capacitor

At the output of a linear voltage regulator a capacitor (“Output Capacitor”) needs to be connected. Depending on the implemented control loop concept, it acts either as simple buffer, or is in addition even part of the control loop and plays therefore an important role in terms of stability.

In terms of control loop’s reaction time, as a simple qualitative approach, it can be summarized that - similar to the above mentioned capacitances - higher capacitance values of the output capacitor cause slower reaction times of the control loop.

3.3 Consequences for the Application

We have seen so far that the reaction time of a linear voltage regulator’s control loop is caused by delays resulting from different capacitances. It was also shown that this reaction time causes variations on the voltage regulator’s output voltage at the moment of current transients. Now, let’s concentrate on the consequences that these voltage variations have within an application.

Potential Malfunction of Load

Every load connected to a linear voltage regulator’s output has a specified operating range. Let’s take as example Infineon’s XC2000 microcontrollers: They specify proper operation for the “Upper Voltage Range” within a supply voltage range between 4.5V..5.5V. In case the supply voltage, that is the linear voltage regulator’s output voltage, is outside this range even for short time, proper operation is not ensured any more. A reliable supply behaviour is shown in [Figure 8](#).

Theoretical Background on Ultra-Low Quiescent Current Control Loop Concepts

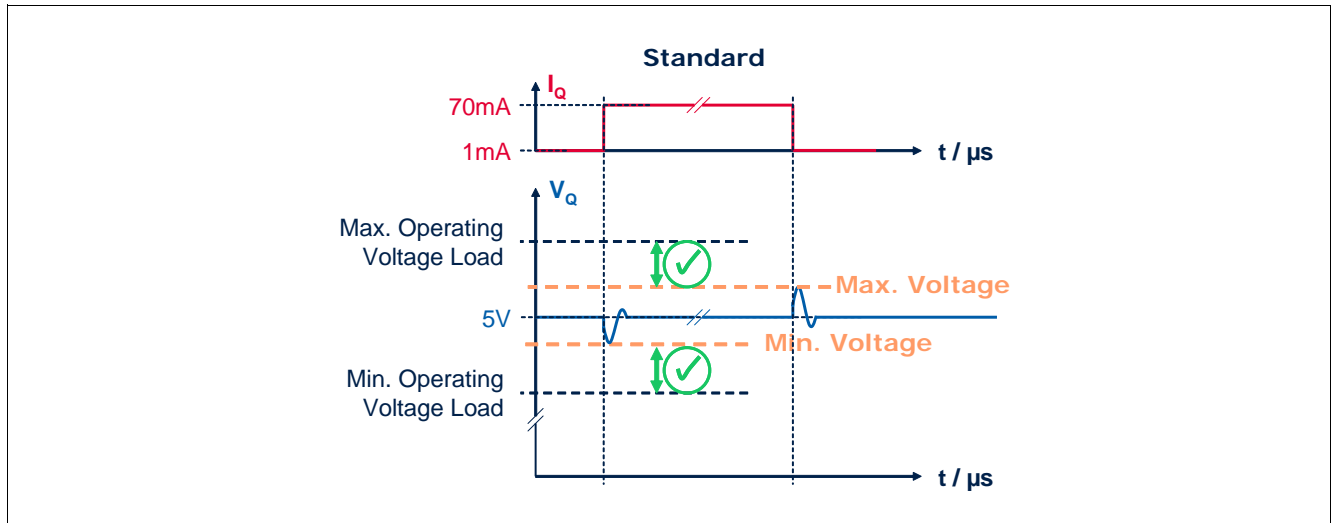


Figure 8 Reliable Supply, Voltage Variation at Current Transients within Load’s Operating Range

Potential Damage of Load

Another painful, but least probable consequence might happen when the voltage variations of the load’s supply are exceeding its absolute maximum ratings. For example, many microcontrollers have 6 V as absolute maximum voltage specified; in this case, any voltage peak higher than 6 V on the supply voltage must be avoided. However, as the absolute maximum ratings are always at least as high as the maximum value of the operating range, the occurrence of this effect is less probable. **Figure 9** shows, how the supply voltage should be.

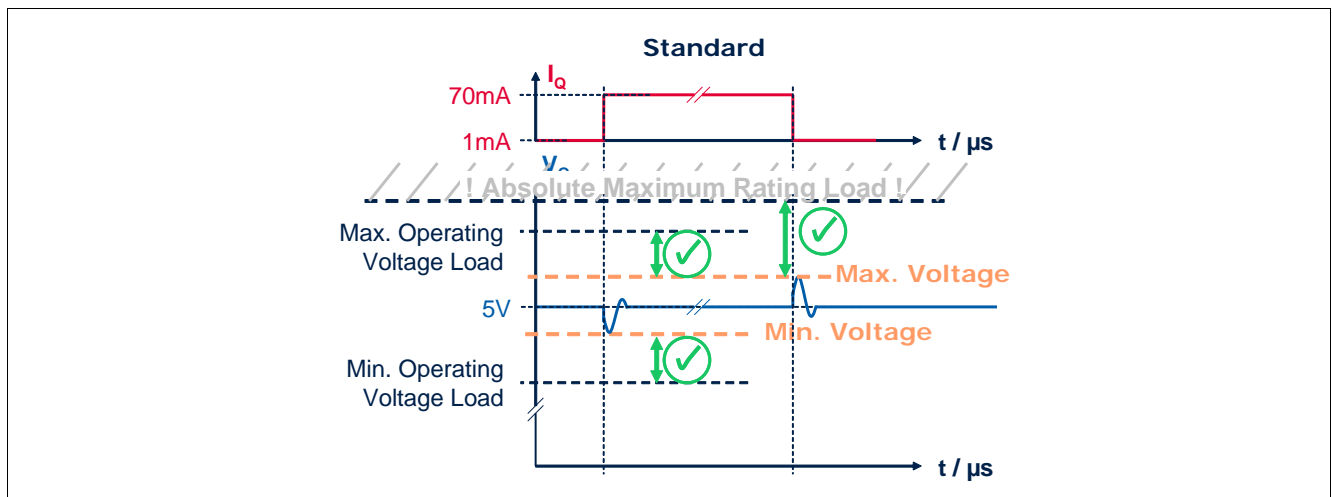


Figure 9 Reliable Supply, Voltage Variation at Current Transients within Load’s Operating Range and below its Absolute Maximum Rating

Most Probable when Voltage Monitoring Present: Unwanted Reset Triggered

The two previously mentioned cases are not necessarily detected at the moment of their occurrence, except if the load is completely damaged. Compared to this, the effect of high voltage variations on the voltage regulator’s output voltage is most probably seen, when a circuit monitoring the voltage is integrated and the voltage variations lead to voltage drops below the monitoring threshold.

Theoretical Background on Ultra-Low Quiescent Current Control Loop Concepts

This can be e.g. a Reset feature integrated in the voltage regulator. In this case, an additional pin on the voltage regulator is connected to a supplied microcontroller’s RST pin. When the monitored voltage (= voltage regulator’s output voltage = microcontroller’s supply voltage) falls below the Reset Threshold, the additional pin resets the microcontroller. This can also happen for short voltage drops at current transients: When the voltage drop at a current transient is too high and falls below the Reset Threshold, an (unwanted) reset is triggered. **Figure 10** illustrates an acceptable voltage drop at a current transient.

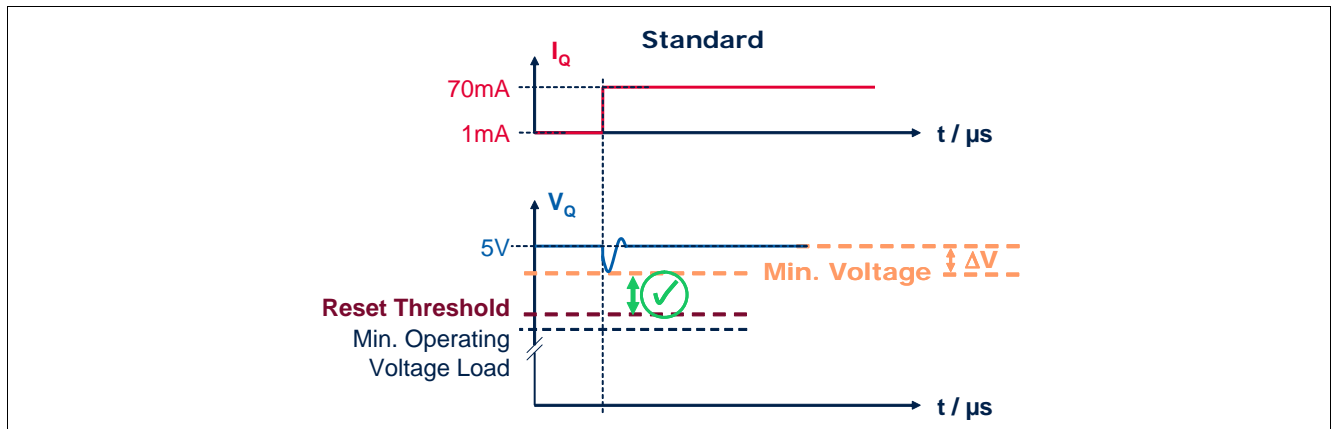


Figure 10 Reliable Supply, Voltage Drop at Current Transient above Reset Threshold

3.4 Influence of the Output Capacitor

So far, we have seen why voltage variations at a voltage regulator’s output voltage can occur at current transients and what are potential consequences then. But we still don’t know yet what can be done to prevent these consequences. Therefore, let’s now focus on the influence of the voltage regulator’s output capacitor.

As mentioned earlier, at the output of a linear voltage regulator a capacitor needs to be connected. We’ve heard that - depending on the implemented control loop concept - this output capacitor acts either as simple buffer, or is in addition even a part of the control loop and plays therefore an important role regarding the loop’s stability. Infineon’s voltage regulators that implement these concepts, specify a min. value for the output capacitor that is at least required, and a range for its parasitic series resistor (“Equivalent Series Resistance” = “ESR”) that has to be respected to maintain stable regulation. **Figure 11** shows this specification for the TLE7273-2.

4.2 Functional Range		Symbol	Limit Values		Unit	Remarks
Pos.	Parameter		Min.	Max.		
4.2.1	Input Voltage	V_I	5.5	45	V	TLE7273-2GV50, TLE7273-2EV50
4.2.2			4.2	45	V	TLE7273-2GV33
4.2.3			4.5	45	V	TLE7273-2GV26
4.2.4	Output Capacitor’s Requirements for Stability	C_O	470	-	nF	-1)
4.2.5		$ESR(C_O)$	-	3	Ω	-2)

1) the minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%
 2) relevant ESR value at $f = 10$ kHz

Figure 11 Specification of Requirements for TLE7273-2’s Output Capacitor

These specified requirements for the output capacitor need to be respected at all times.

Theoretical Background on Ultra-Low Quiescent Current Control Loop Concepts

Apart from this, as the capacitor acts always as a buffer, it has always a direct influence on the voltage variation at load steps. Let's now see why.

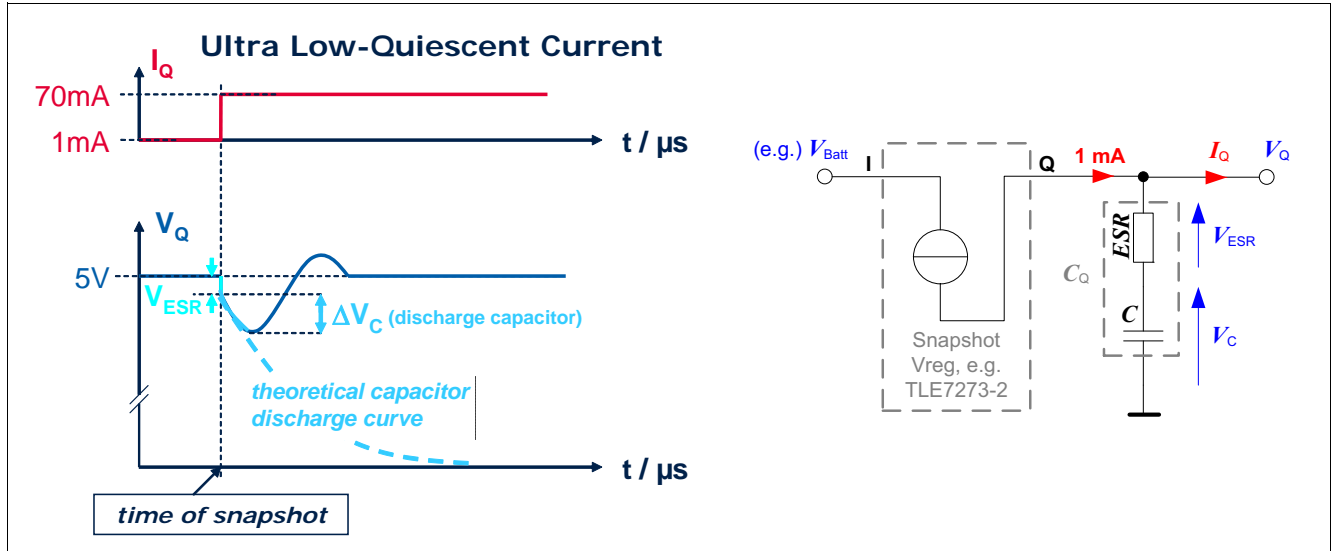


Figure 12 Equivalent Circuit for Snapshot of Linear Voltage Regulator at Current Transient

Figure 12 shows at the left side again the voltage variation at a current transient for an ultra-low quiescent current linear voltage regulator. The equivalent circuit at the right side shows a snapshot of the voltage regulator at the moment the current transient occurs. At this point, the voltage regulator doesn't recognize the transient yet and can be modelled by a current source adjusted to the previous current, for our example to 1 mA. Nearly all current (70 mA - 1 mA) needs therefore to be sourced by the output capacitor C_q . As every capacitor contains an ESR, at the output voltage a small immediate drop can be recognized at this point. Then, as long as the voltage regulator's control loop doesn't react yet, C_q still needs to source nearly all current (70 mA - 1 mA), the output voltage has therefore the shape of a typical capacitor discharge curve during this period and is dropping by ΔV_C .

It is now obvious that increasing the capacitance value of C_q leads to a smaller voltage variation because of a smaller ΔV_C . This ΔV_C is smaller as a bigger capacitor buffers more energy and is discharged more slowly. This is shown in **Figure 13**.

Just to mention, it can be also seen in this figure, what we heard in **Chapter 3.2**: Increasing the output capacitance increases the control loop's reaction time. This means, even if increasing the capacitance value leads to smaller voltage variations, the relation between capacitance and voltage variation is not proportional, e.g. the double of the capacitor's size does not lead to half of the voltage variation, its still more than a half.

Theoretical Background on Ultra-Low Quiescent Current Control Loop Concepts

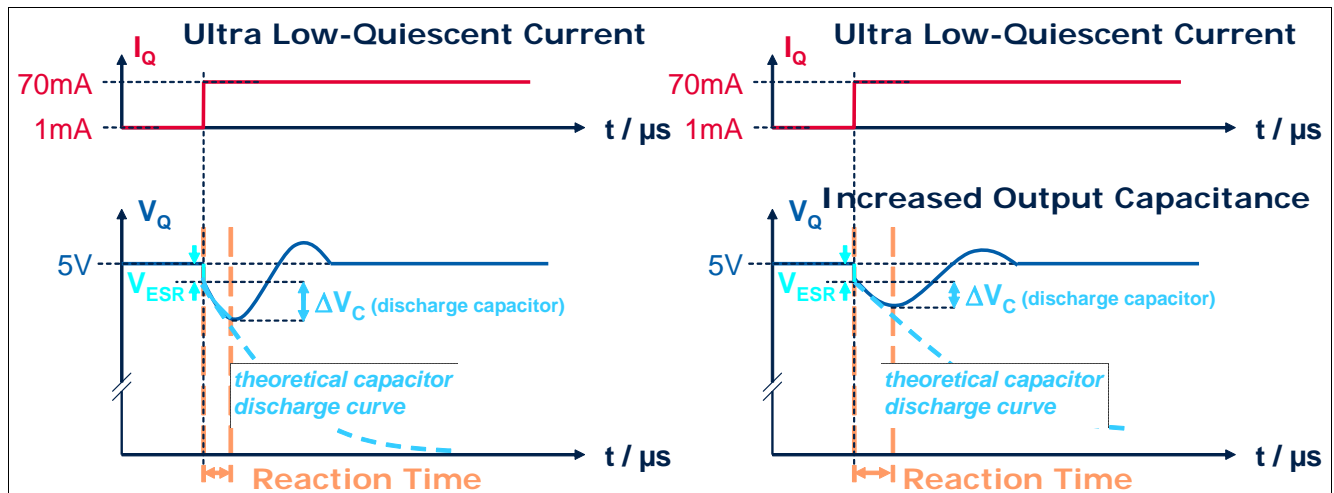


Figure 13 Comparison Variation of Output Voltage at Current Transient for Different Output Capacitance Values

Generally speaking, higher capacitance values will always lower the voltage variations. This is especially important to keep in mind for ultra-low quiescent current linear voltage regulators, as their control loop is optimized for ultra-low quiescent current and shows a slower reaction time due to very small bias currents. Hence, for an application requiring ultra-low quiescent current, the output capacitor of the linear voltage regulator has to be sized accordingly, not only to fulfill the voltage regulator’s requirements in terms of stability, but also to buffer sufficiently the worst-case current transients within the application.

3.5 Conclusion

Let’s summarize what we have seen so far:

- Control loop’s reaction time at current transients influences the linear voltage regulator’s output voltage: The faster the reaction time, the smaller variations of the output voltage.
- Control loop’s reaction time is caused by delays within the silicon. It depends therefore on the capacitance values of integrated capacitors respectively parasitic effects and the bias currents. The higher the capacitances and the lower the bias currents, the longer the delays and the reaction time.
- Potential risks of too high voltage variations are: 1. triggering unwanted Reset, 2. malfunction of supplied microcontroller by exceeding its specified operating range, 3. damage of load by exceeding its max. ratings.
- Output capacitor of linear voltage regulator buffers output voltage at current transients: Increasing the capacitance lowers the voltage variations at current transients and avoids the mentioned risks when dimensioned correctly.

From this information, we can conclude:

Keeping the quiescent current at a linear voltage regulator ultra-low and at the same time the output capacitor very small, is physically contradicting, as these regulators must have very low bias currents to keep the current consumption ultra-low. Therefore, at current transients, the control loop’s reaction time is always slower and the voltage variations are always higher than at a standard linear voltage regulator. Thus, one needs to pay attention, when these voltage regulators are used in an application where big current transients can occur: Even if a control loop concept is implemented that requires only small capacitors to maintain loop stability, higher capacitance values might be needed to buffer big current transients and avoid risks like unwanted resets or malfunction of supplied microcontrollers.

4 Dimensioning the Output Capacitor of an Ultra-Low Quiescent Current Voltage Regulator

Infineon's ultra-low quiescent current voltage regulators combine the ultra-low quiescent current concept with a MOSFET power stage. This offers the lowest possible current consumption even at sophisticated feature sets and requires only very small output capacitance values for the control loop's stability (TLE7273-2: $C_Q \geq 470$ nF). Another advantage of the MOSFET power stage is that the current consumption remains ultra-low even at high output currents.

Due to this ultra-low quiescent current concept, the control loop's reaction on current transients is slower than for standard voltage regulators. This correlation is demonstrated in [Chapter 3](#). When these voltage regulators are used in applications where big current transients can occur, e.g. at the transition from stand-by to normal operation, high voltage variations at the voltage regulators' output voltage with consequences on the application (see [Chapter 3.3](#)) might result.

To avoid these high voltage variations, basically two solutions are possible:

1. Avoid big current transients wherever possible.
2. Increase the output capacitor to buffer the voltage regulator's output voltage.

In the following we will first provide hints on 1., how to avoid big current transients, then focus on 2. and provide a method to dimension the output capacitor correctly.

4.1 How to Avoid Big Current Transients

To keep the output capacitor's size as small as possible, one should first of all try to avoid big current transients within the application. As the most critical transients appear at the start up or at the transition from standby to normal operation, here several recommendations:

- Many microcontrollers provide solutions for a so-called "soft-start", the different blocks are then started step by step; if possible for your application, apply this kind of start up.
- If your microcontroller doesn't implement a "soft-start", try to manually implement delays during the microcontroller's start up and avoid a start of all blocks at the same time.
- Switch off I/Os by default when starting the microcontroller and switch them on step by step after a delay.
- If several loads are present in the application, switch them on step by step after a delay.

4.2 How to Dimension the Output Capacitor

Step 1: Check for Worst-Case Current Transients within Application

As mentioned above, first make sure to avoid big current transients as much as possible. When this is ensured, the worst-case current transients within the application need to be evaluated. A "worst-case" current transient is a high transient starting at very low currents < 5 mA.

It can be estimated, when a detailed documentation of all loads is available. It would be then mostly at the transition from stand-by (very low current) to normal operation (high current), when several loads are switched on at the same time.

The more realistic (and mostly easier) way is to measure it at the bench. For this, run the application and watch either the overall supply current or - if possible - the voltage regulator's output current as well as its output voltage at the scope (see [Figure 14](#)). At this time, connect as output capacitor a type that just respects the minimum values required for stability, no need to consider its buffer effect yet. Try to run all possible

Dimensioning the Output Capacitor of an Ultra-Low Quiescent Current Voltage

application conditions and note the current transients caused by their transitions. As mentioned, note especially high current transients starting at very small currents < 5 mA, these are generally the most critical.

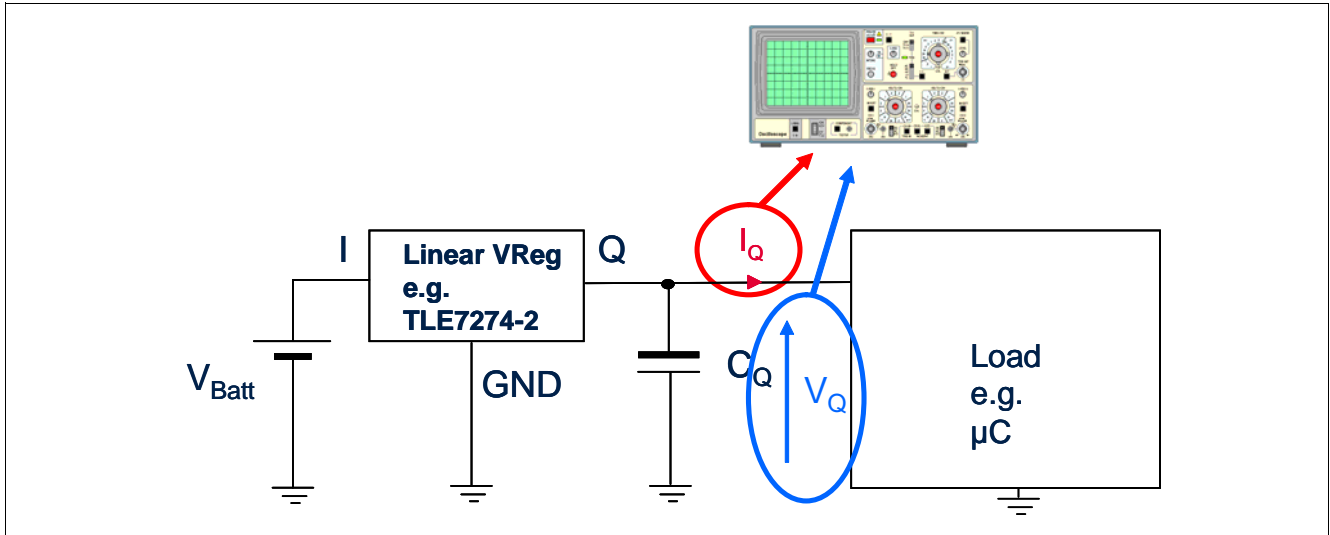


Figure 14 Measurement Setup for Evaluation of Worst Case Current Transients

Step 2: Define Maximum Allowed Voltage Variation ΔV_{\max} at Current Transient

Now, you need to define, which maximum voltage variation at a worst case current transient is allowed within your application. As this definition strongly depends on the application, we concentrate here on providing generic hints:

In case you have an undervoltage monitor, e.g. Reset, implemented, its threshold voltage might be a target as minimum voltage to maintain. Example: Let's assume an implemented Reset with a threshold at max. 4.8 V for a 5 V supply voltage, a target for the maximum allowed voltage variation would be $\Delta V_{\max} = 5 \text{ V} - 4.8 \text{ V} = 200 \text{ mV}$.

Another parameter that should be considered is the operating range of connected loads. As a malfunction of the load could be a consequence, its operating range should not be exceeded. Example: The min. operating voltage of a connected microcontroller is at 4.5 V. When supplying it with 5 V and no undervoltage monitor present, a target for the maximum allowed voltage variation would be $\Delta V_{\max} = 5 \text{ V} - 4.5 \text{ V} = 500 \text{ mV}$.

In **Figure 15** both scenarios are shown.

In any case, we recommend to consider within your maximum voltage variation a reasonable safety margin.

Dimensioning the Output Capacitor of an Ultra-Low Quiescent Current Voltage

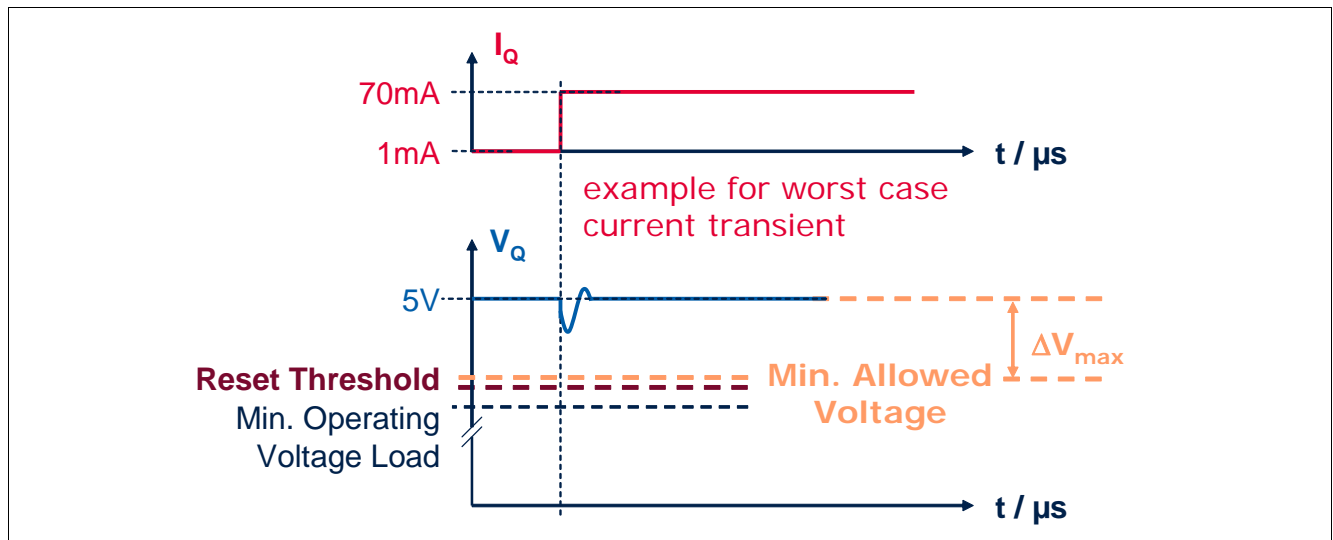


Figure 15 Example for Definition of the Maximum Allowed Voltage Variation ΔV_{max}

Step 3: Select Output Capacitor

Now we know the “worst-case” current transient as well as the max. allowed voltage variation. With this information, the graphs in “**Typ. Perf. Characteristics Output Voltage Variation ΔV_Q vs. Output Current Transient ΔI_Q** ” on Page 19 can be used as guideline for selecting the right capacitor. These graphs show for different output capacitors the relation between voltage variation ΔV_Q and current transient ΔI_Q , using different start currents as a parameter. They were generated for all of Infineon’s ultra-low quiescent current voltage regulators that are available today and are therefore valid for:

- TLE7270-2
- TLE7272-2
- TLE7273-2
- TLE7274-2
- TLE7276-2
- TLE7278-2
- TLE7279-2

Note: As the worst-case for the voltage regulator is at high temperature and as current transients won't happen at $T_j = -40^\circ\text{C}$, graphs are provided for two temperatures each, $T_j = 25^\circ\text{C}$ and $T_j = 150^\circ\text{C}$.

Let's take an example to see how to work with these graphs:

We assume as worst-case current transient 0.5 mA to 60 mA and a max. allowed voltage variation of 200 mV. Furthermore, let's say that the voltage regulator can reach at the worst-case transient high temperatures. With this information, we concentrate only on the graphs where $T_j = 150^\circ\text{C}$. At all these graphs, we need to consider only the curve with $I_{Q1} = 0.5\text{ mA}$ as a parameter, as our worst-case transient starts at 0.5 mA. Start at the curve for a 470 nF capacitor. At the considered curve, check at 60 mA whether the voltage variation is less than 200mV. If not, go on with the curve for the next capacitor and do the check again, otherwise you have found a potentially suitable capacitor for your application and can proceed with Step 4. This example is illustrated in **Figure 16**.

Dimensioning the Output Capacitor of an Ultra-Low Quiescent Current Voltage

Step 4: Verify Selected Output Capacitor within Application

After having selected a potential output capacitor, you should solder it in the application and run it again at all possible conditions, like done at Step 1. Watch again the supply current / voltage regulator's output current and its output voltage with the scope like shown in **Figure 14**. In case the voltage variation stays within your defined maximum value, the selected capacitor is the right one. Otherwise, go for the next higher capacitor value and do the verification test again.

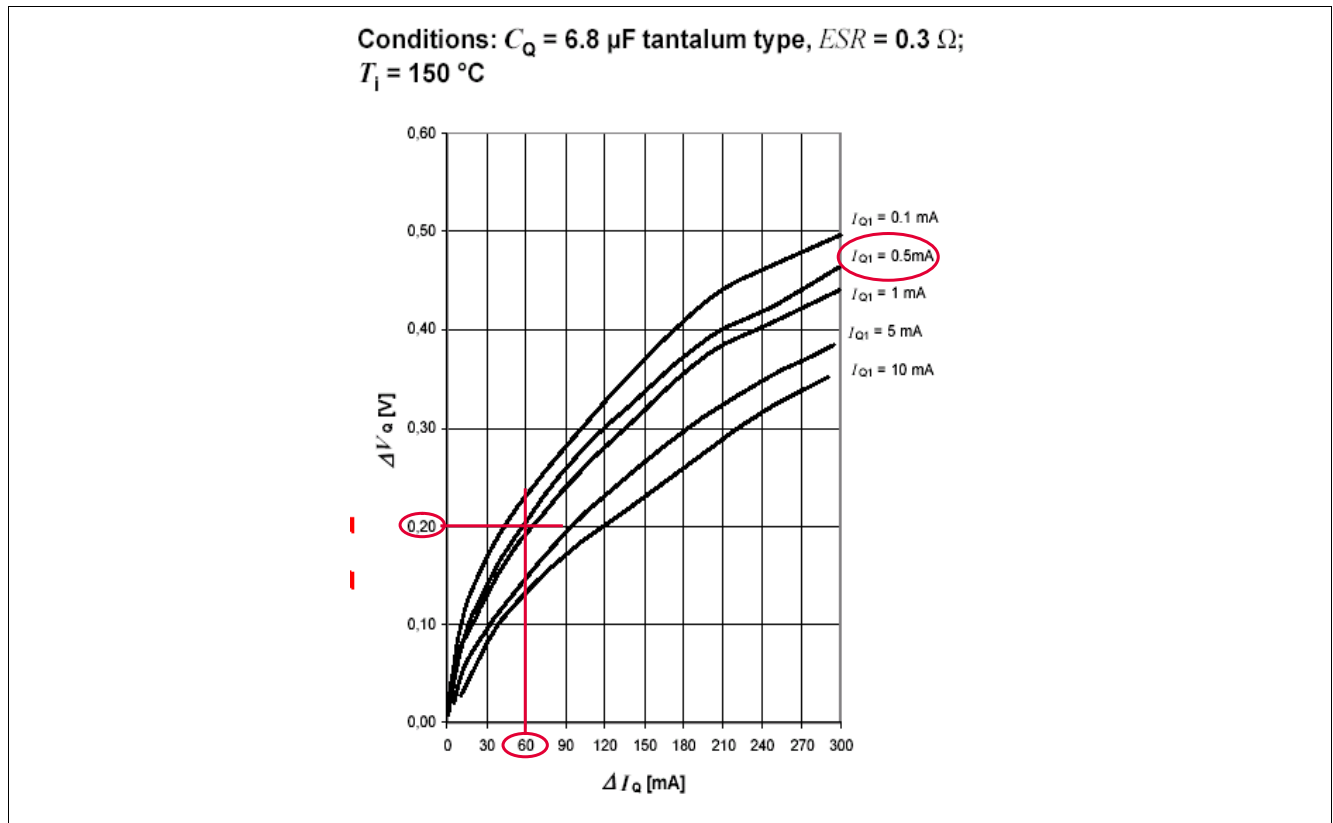


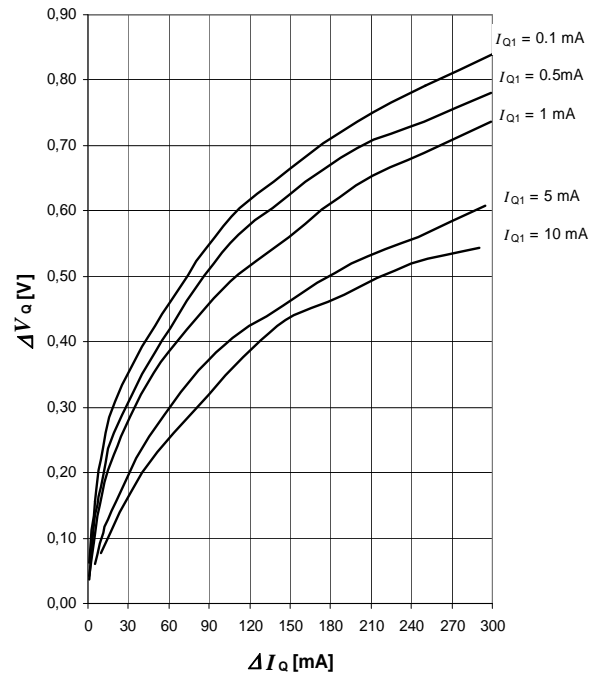
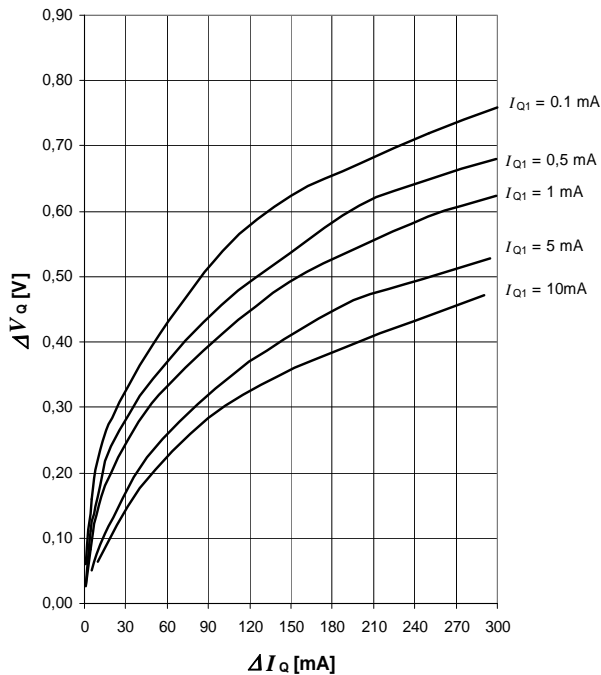
Figure 16 Example for Selection of a Suitable Capacitor Using the Below Graphs

Dimensioning the Output Capacitor of an Ultra-Low Quiescent Current Voltage

Typ. Perf. Characteristics Output Voltage Variation ΔV_Q vs. Output Current Transient ΔI_Q ¹⁾

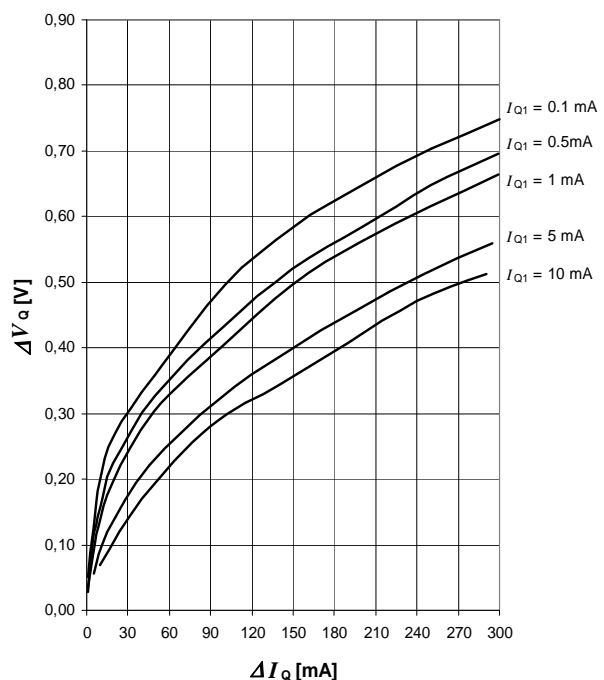
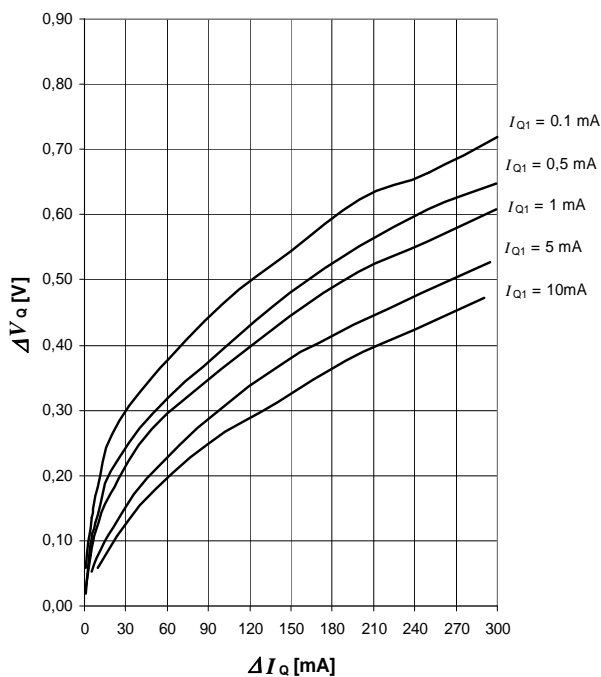
Conditions: $C_Q = 470$ nF ceramic type; $T_j = 25$ °C

Conditions: $C_Q = 470$ nF ceramic type; $T_j = 150$ °C



Conditions: $C_Q = 1$ μF ceramic type; $T_j = 25$ °C

Conditions: $C_Q = 1$ μF ceramic type; $T_j = 150$ °C

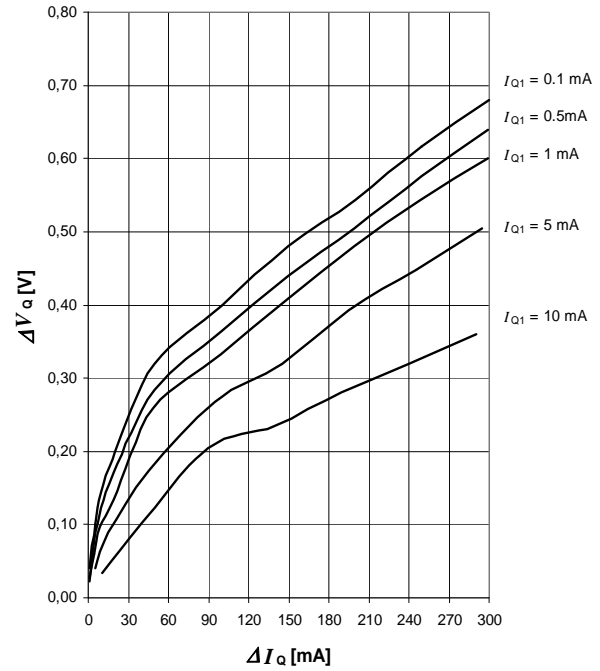
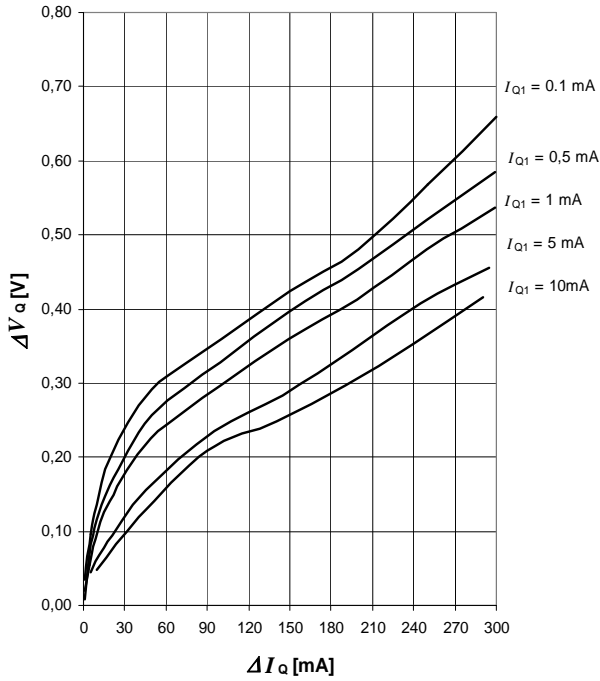


Dimensioning the Output Capacitor of an Ultra-Low Quiescent Current Voltage

Typ. Perf. Characteristics Output Voltage Variation ΔV_Q vs. Output Current Transient ΔI_Q ¹⁾

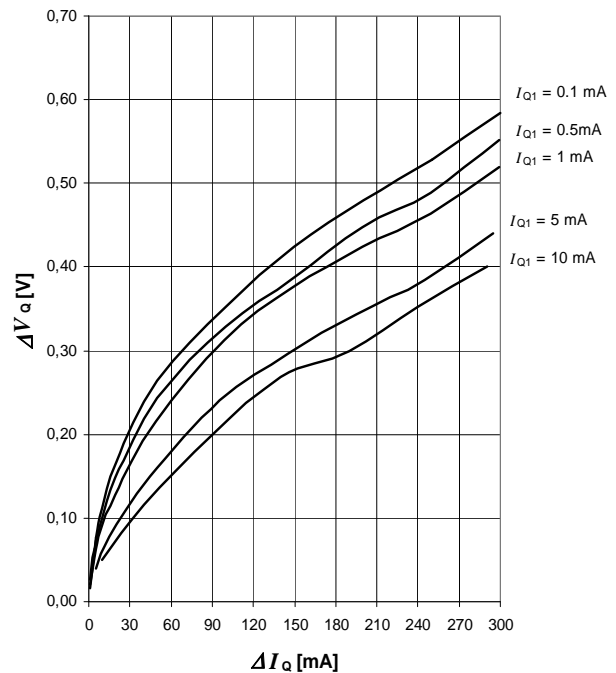
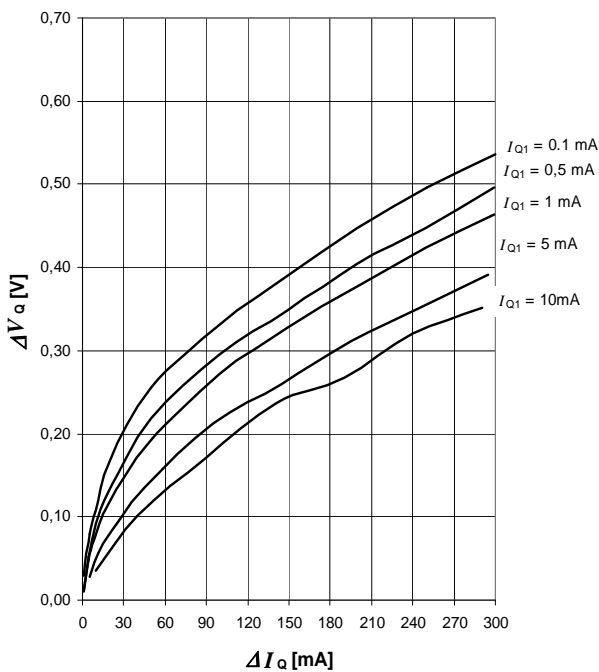
Conditions: $C_Q = 2.2 \mu\text{F}$ ceramic type; $T_j = 25^\circ\text{C}$

Conditions: $C_Q = 2.2 \mu\text{F}$ ceramic type; $T_j = 150^\circ\text{C}$



Conditions: $C_Q = 4.7 \mu\text{F}$ ceramic type; $T_j = 25^\circ\text{C}$

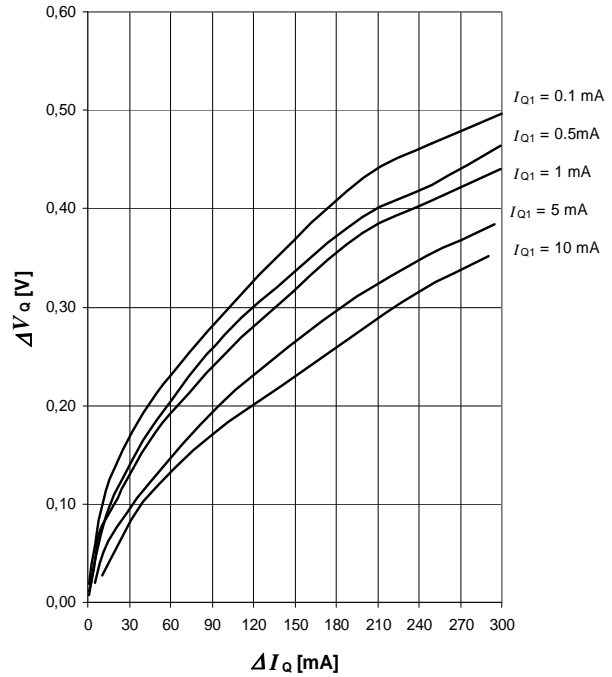
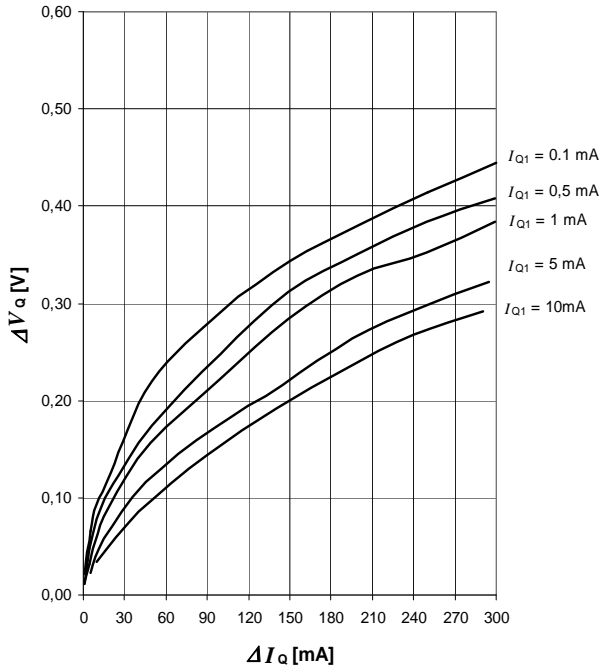
Conditions: $C_Q = 4.7 \mu\text{F}$ ceramic type; $T_j = 150^\circ\text{C}$



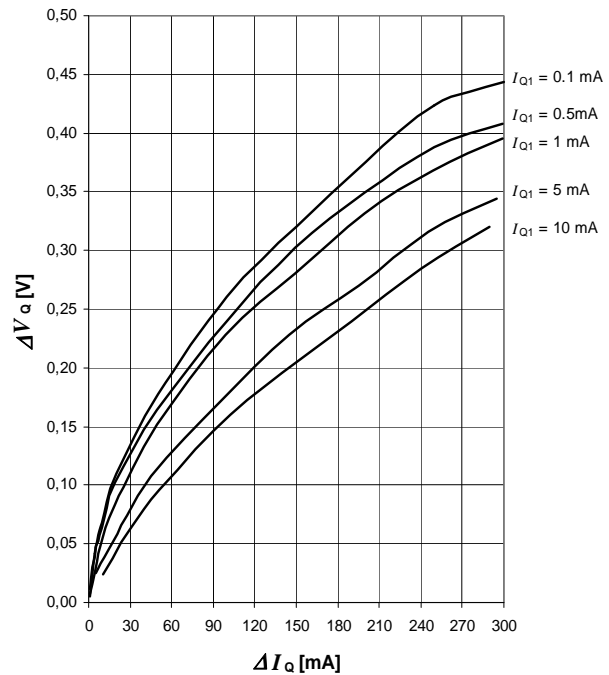
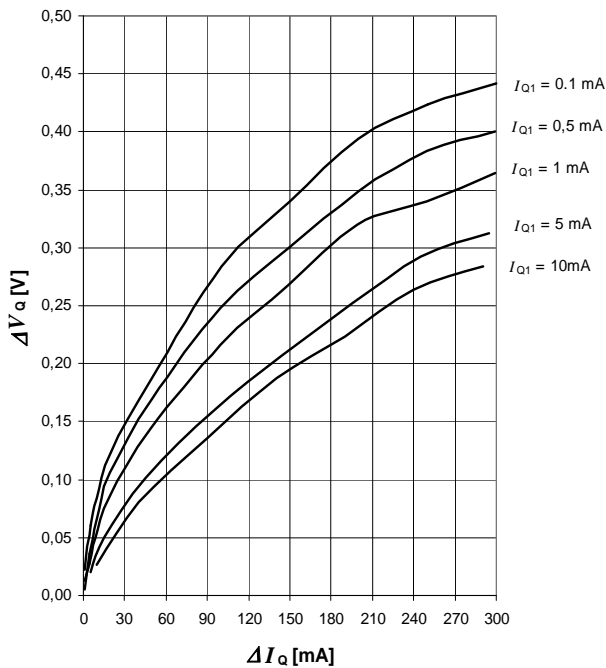
Dimensioning the Output Capacitor of an Ultra-Low Quiescent Current Voltage

Typ. Perf. Characteristics Output Voltage Variation ΔV_Q vs. Output Current Transient ΔI_Q ¹⁾

Conditions: $C_Q = 6.8 \mu\text{F}$ tantalum type, $ESR = 0.3 \Omega$; $T_j = 25^\circ\text{C}$ **Conditions: $C_Q = 6.8 \mu\text{F}$ tantalum type, $ESR = 0.3 \Omega$; $T_j = 150^\circ\text{C}$**



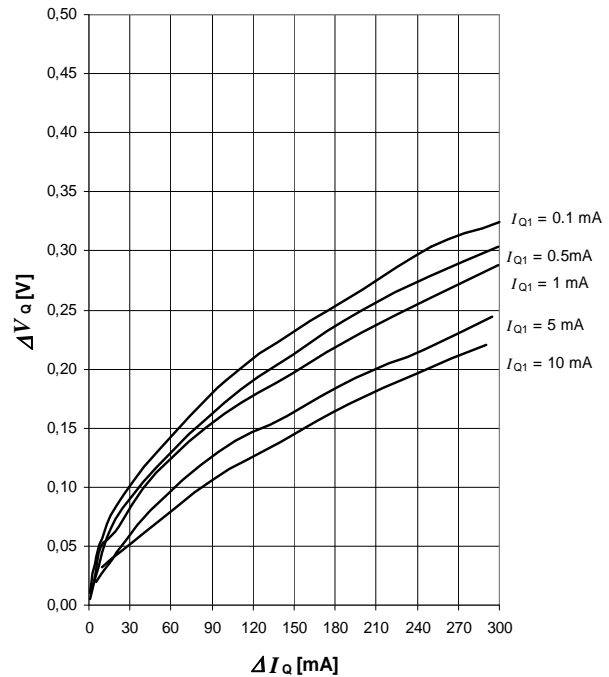
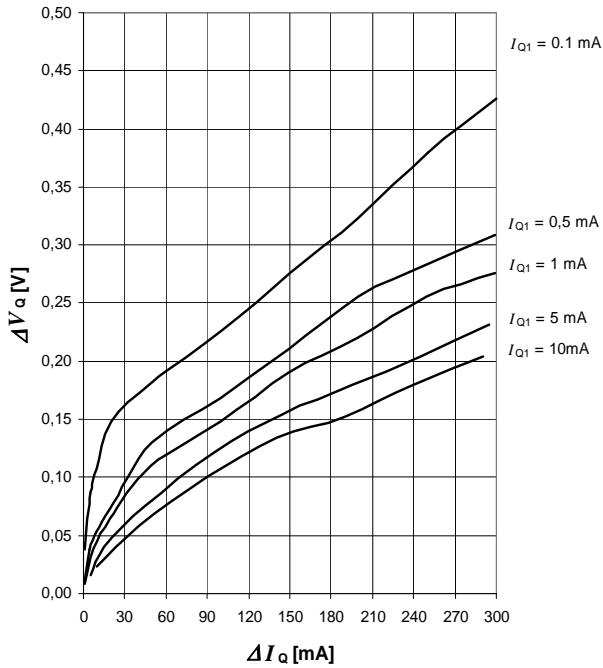
Conditions: $C_Q = 10 \mu\text{F}$ tantalum type, $ESR = 0.26 \Omega$; $T_j = 25^\circ\text{C}$ **Conditions: $C_Q = 10 \mu\text{F}$ tantalum type, $ESR = 0.26 \Omega$; $T_j = 150^\circ\text{C}$**



Dimensioning the Output Capacitor of an Ultra-Low Quiescent Current Voltage

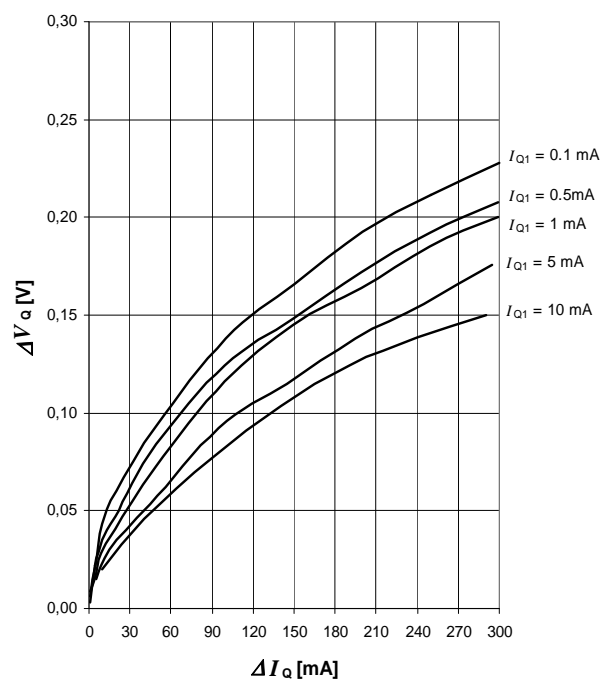
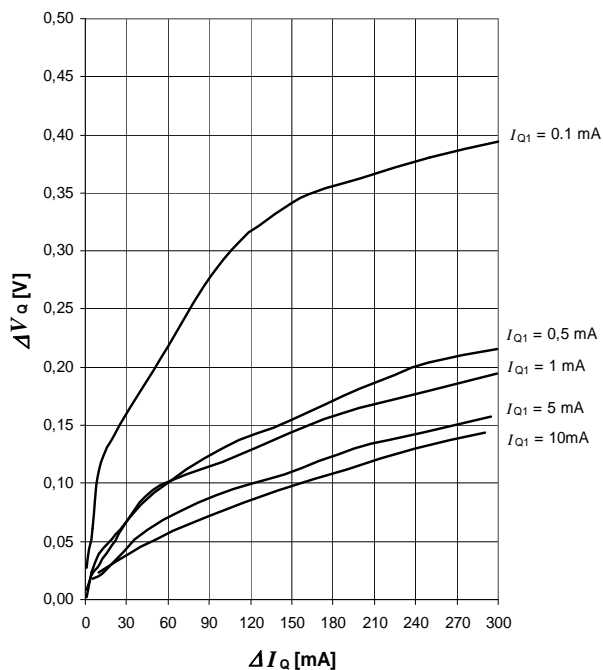
Typ. Perf. Characteristics Output Voltage Variation ΔV_Q vs. Output Current Transient ΔI_Q ¹⁾

Conditions: $C_Q = 22 \mu\text{F}$ tantalum type, $ESR = 0.26 \Omega$; $T_j = 25^\circ\text{C}$ **Conditions: $C_Q = 22 \mu\text{F}$ tantalum type, $ESR = 0.26 \Omega$; $T_j = 150^\circ\text{C}$**



Conditions: $C_Q = 47 \mu\text{F}$ tantalum type, $ESR = 0.3 \Omega$; $T_j = 25^\circ\text{C}$

Conditions: $C_Q = 47 \mu\text{F}$ tantalum type, $ESR = 0.3 \Omega$; $T_j = 150^\circ\text{C}$



1) valid for: TLE7270-2, TLE7272-2, TLE7273-2, TLE7274-2, TLE7276-2, TLE7278-2, TLE7279-2

5 Additional Information

Information regarding the product portfolio of Linear Voltage Regulators with ultra-low quiescent current as well as the related data sheets containing the product information and specification can be found on our webpage: <http://www.infineon.com>.

Revision History

6 Revision History

Revision	Date	Changes
1.01	2014-09-26	Infineon Style Guide update; Editorial changes
1.0	2009-09-30	Initial document

Trademarks of Infineon Technologies AG

AURIX™, C166™, CanPAK™, CIPOS™, CIPURSE™, CoolGaN™, CoolMOS™, CoolSET™, CoolSiC™, CORECONTROL™, CROSSAVE™, DAVE™, DI-POL™, DrBLADE™, EasyPIM™, EconoBRIDGE™, EconoDUAL™, EconoPACK™, EconoPIM™, EiceDRIVER™, eupec™, FCOS™, HITFET™, HybridPACK™, ISOFACE™, IsoPACK™, i-Wafer™, MIPAQ™, ModSTACK™, my-d™, NovalithIC™, OmniTune™, OPTIGA™, OptiMOS™, ORIGA™, POWERCODE™, PRIMARION™, PrimePACK™, PrimeSTACK™, PROFET™, PRO-SIL™, RASIC™, REAL3™, ReverSave™, SatRIC™, SIEGET™, SIPMOS™, SmartLEWIS™, SOLID FLASH™, SPOC™, TEMPFET™, thinQ!™, TRENCHSTOP™, TriCore™.

Other Trademarks

Advance Design System™ (ADS) of Agilent Technologies, AMBA™, ARM™, MULTI-ICE™, KEIL™, PRIMECELL™, REALVIEW™, THUMB™, µVision™ of ARM Limited, UK. ANSI™ of American National Standards Institute. AUTOSAR™ of AUTOSAR development partnership. Bluetooth™ of Bluetooth SIG Inc. CAT-iq™ of DECT Forum. COLOSSUS™, FirstGPS™ of Trimble Navigation Ltd. EMV™ of EMVCo, LLC (Visa Holdings Inc.). EPCOS™ of Epcos AG. FLEXGO™ of Microsoft Corporation. HYPERTERMINAL™ of Hilgraeve Incorporated. MCS™ of Intel Corp. IEC™ of Commission Electrotechnique Internationale. IrDA™ of Infrared Data Association Corporation. ISO™ of INTERNATIONAL ORGANIZATION FOR STANDARDIZATION. MATLAB™ of MathWorks, Inc. MAXIM™ of Maxim Integrated Products, Inc. MICROTEC™, NUCLEUS™ of Mentor Graphics Corporation. MIPI™ of MIPI Alliance, Inc. MIPS™ of MIPS Technologies, Inc., USA. muRata™ of MURATA MANUFACTURING CO., MICROWAVE OFFICE™ (MWO) of Applied Wave Research Inc., OmniVision™ of OmniVision Technologies, Inc. Openwave™ of Openwave Systems Inc. RED HAT™ of Red Hat, Inc. RFMD™ of RF Micro Devices, Inc. SIRIUS™ of Sirius Satellite Radio Inc. SOLARIS™ of Sun Microsystems, Inc. SPANSION™ of Spansion LLC Ltd. Symbian™ of Symbian Software Limited. TAIYO YUDEN™ of Taiyo Yuden Co. TEAKLITE™ of CEVA, Inc. TEKTRONIX™ of Tektronix Inc. TOKO™ of TOKO KABUSHIKI KAISHA TA. UNIX™ of X/Open Company Limited. VERILOG™, PALLADIUM™ of Cadence Design Systems, Inc. VLYNQ™ of Texas Instruments Incorporated. VXWORKS™, WIND RIVER™ of WIND RIVER SYSTEMS, INC. ZETEX™ of Diodes Zetex Limited.

Trademarks Update 2014-07-17

www.infineon.com

Edition 2014-09-26

Published by

Infineon Technologies AG

81726 Munich, Germany

© 2014 Infineon Technologies AG.

All Rights Reserved.

Do you have a question about any aspect of this document?

Email: erratum@infineon.com

Document reference

Doc_Number

Legal Disclaimer

THE INFORMATION GIVEN IN THIS APPLICATION NOTE (INCLUDING BUT NOT LIMITED TO CONTENTS OF REFERENCED WEBSITES) IS GIVEN AS A HINT FOR THE IMPLEMENTATION OF THE INFINEON TECHNOLOGIES COMPONENT ONLY AND SHALL NOT BE REGARDED AS ANY DESCRIPTION OR WARRANTY OF A CERTAIN FUNCTIONALITY, CONDITION OR QUALITY OF THE INFINEON TECHNOLOGIES COMPONENT. THE RECIPIENT OF THIS APPLICATION NOTE MUST VERIFY ANY FUNCTION DESCRIBED HEREIN IN THE REAL APPLICATION. INFINEON TECHNOLOGIES HEREBY DISCLAIMS ANY AND ALL WARRANTIES AND LIABILITIES OF ANY KIND (INCLUDING WITHOUT LIMITATION WARRANTIES OF NON-INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS OF ANY THIRD PARTY) WITH RESPECT TO ANY AND ALL INFORMATION GIVEN IN THIS APPLICATION NOTE.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office. Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.