AN2007-04

How to calculate and minimize the dead time requirement for IGBTs properly

Power Management and Drives

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Revision History:	2007-08	V1.0
Previous Version:	none	
Page	Subjects (major changes since last revision)	
	First release	

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1 Introduction

In modern industry the voltage source inverter with IGBT devices is used more and more. To ensure proper operation, the bridge shoot through always should be avoided. Bridge shoot through will generate unwanted additional losses or even cause thermal runaway. As a result failure of IGBT devices and whole inverter is possible.

1.1 Reason of IGBT bridge shoot through

The typical configuration of a phase-leg with IGBTs is shown in the following figure. In normal operation two IGBTs will be switched on and off one after the other. Having both devices conducting at the same time will result in a rise of current only limited by DC-link stray inductance.
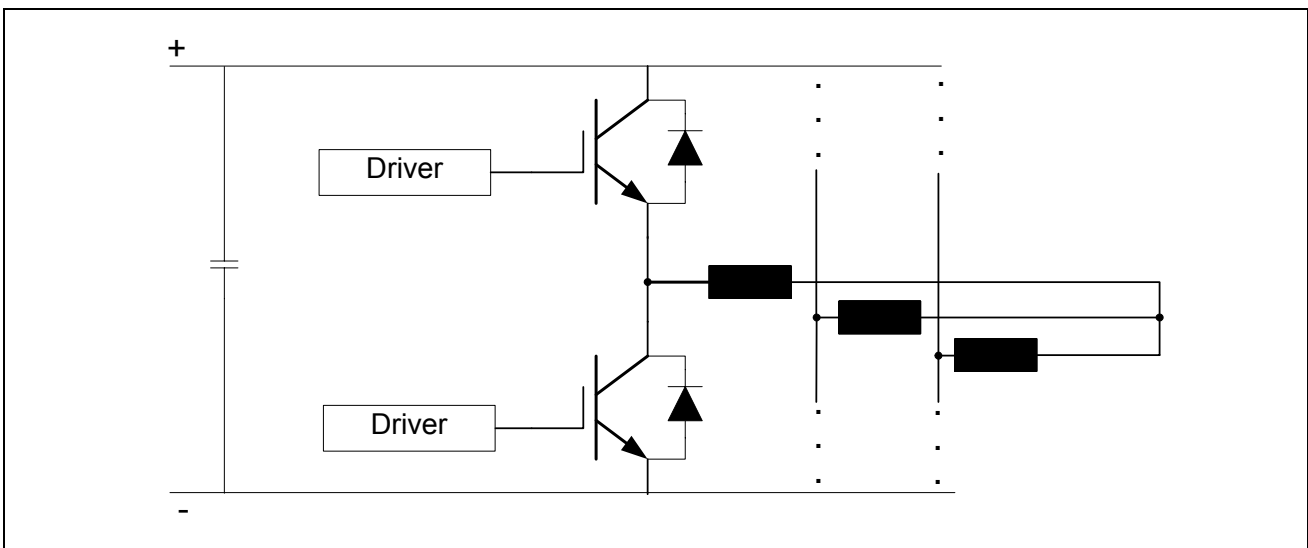

Figure 1   Typical configuration of a voltage source inverter

Of course no one will turn on the two IGBTs at the same time on purpose, but since the IGBT is not an ideal switch, turn on time and turn off time are not strictly identical. In order to avoid bridge shoot through it is always recommended to add a so called "interlock delay time" or more popular "dead time" into the control scheme. With this additional time one IGBT will be always turned off first and the other will be turned on after dead time is expired, hence bridge shoot through caused by the unsymmetrical turn on and turn off time of the IGBT devices can be avoided.

1.2 Impact of dead time on inverter operation

Generally there are two types of dead time, the first one is control dead time and the second is effective dead time. The control dead time is the dead time, which will be implemented into control algorithms in order to get proper effective dead time at the devices. Target for setting control dead time is to ensure that effective dead time is always positive. Due to the fact that calculation of control dead time is always based on a worst case consideration, an effective dead time being a significant portion of the control dead time will result.

Providing dead time can on one side avoid bridge shoot through but on the other side it has also adverse effect. To clarify the effect of dead time, let's consider one leg of the voltage source inverter as shown in Figure. 2. Assuming first that output current flows in direction shown on the illustration IGBT T1 switches from ON to OFF and IGBT T2 switches from OFF to ON after slight dead time. During effective dead time both devices are off and freewheeling diode D2 is conducting output current. So negative DC link voltage is applied to the output, which is desired here. Consider the other case that T1 switches from OFF to ON and T2 from ON to OFF, then, with current in the same direction D2 still conducts the current during dead time, so that output voltage will be also negative DC link voltage, which is undesired here. The conclusion can be

summarized as follows: during effective dead time output voltage is determined by the direction of output current but not the control signal.

If we consider output current in the opposite direction than illustrated in figure 2, then we will gain a voltage if T1 switches from ON to OFF and T2 switched from OFF to ON. So in general output voltage and as a result also output current will be distorted with application of a dead time. If we choose a dead time unnecessary large, then in case of an induction motor the system will become instable and may cause some destructive effects [1]. So the process of choosing dead time is very important and should be performed very carefully.
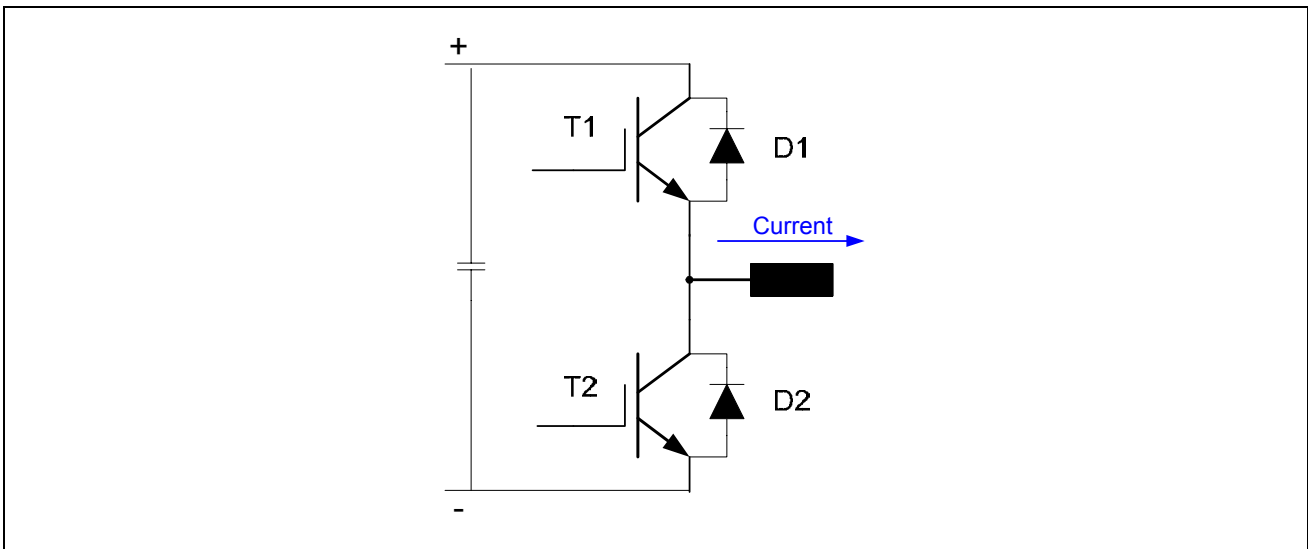

Figure 2   **One leg of voltage source inverter**

This application note will explain how to measure delay time of IGBTs in practice and how to calculate the control dead time properly based on measurements.

2   Calculate proper dead time

As already mentioned, dead time should be chosen on one hand to satisfy the need of avoiding bridge shoot through, on the other hand dead time should be chosen as small as possible to ensure correct operation of voltage source inverter. So a big challenge here is to find out a proper dead time for a dedicated IGBT device and driver.

2.1   Basics for calculating the dead time

For calculation of control dead time we use the following equation:

$$t_{dead} = \left[\left(t_{D\_OFF\_MAX} - t_{D\_ON\_MIN} \right) + \left(t_{PDD\_MAX} - t_{PDD\_MIN} \right) \right] \times 1.2 \qquad (1)$$

Where   Td_off_max   : the maximal turn off delay time.

                        Td_on_min   : the minimal turn on delay time.

                        Tpdd_max   : the maximal propagation delay of driver.

                        Tpdd_min   : the minimum propagation delay of driver.

                        1.2   : safety margin to be multiplied.

In this equation the first term td_off_max-td_on_min is the difference of the maximal turn off delay time and the minimal turn on delay time. This term describes characteristic of IGBT device itself plus gate resistor which is used. Since fall and rise time is normally very short in comparison with delay time, they will be not considered here. The other term tpdd_max-tpdd_min is the propagation delay time difference (delay time

mismatch) which is determined from driver. This parameter will be found normally in datasheet of driver from driver manufacturers. Typically this value is quiet high with opto-coupler based drivers.

Sometimes dead time will be calculated from typical datasheet values just multiplying by a safety factor from field experience. This method will work in some cases but is not precise enough in general. With measurements shown here, a more precise approach will be presented.

Because IGBT datasheet only gives typical values for standardized operation condition, it is necessary to obtain the maximal values for dedicated driving condition. For this purpose a series of measurements is done in order to obtain proper value for delay time and then to calculate dead time.

2.2   Definition of switching and delay times

Since we will talk a lot about switching and delay times, it is necessary to give a clear definition here.

Infineon Technologies defines the switching time of IGBT as follows:

t_{d_on} : from 10% of V_{ge} to 10% if I_c.

t_r : from 10% of I_c to 90% of I_c.

t_{d_off} : from 90% of V_{ge} to 90% of I_c.

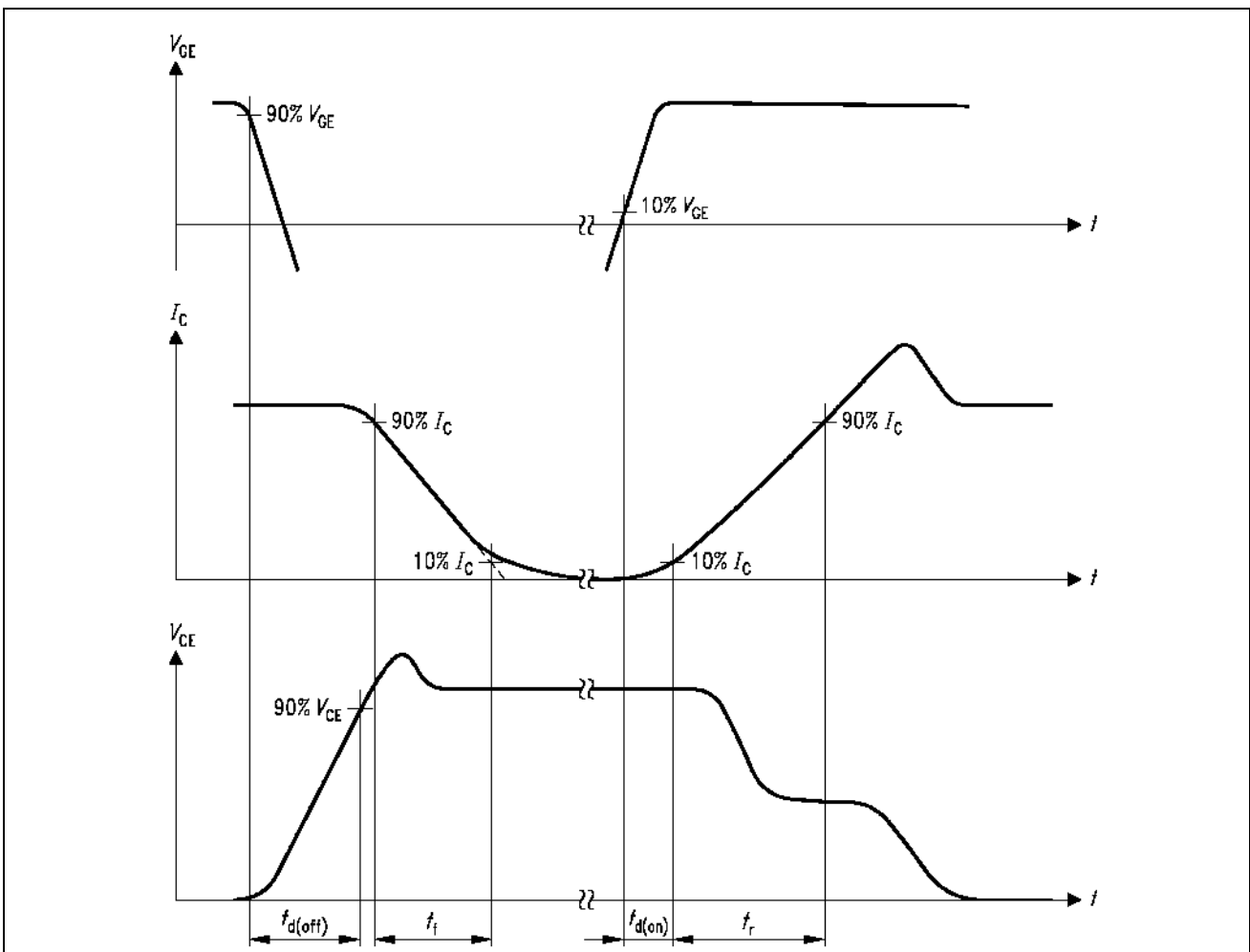t_f : from 90% of I_c to 10% of I_c.

Figure 3   Definition of switching times.

2.3 Influence of gate resistor / driver output impedance

The choice of gate resistor will have significant impact on switching delay time. Generally to say, the larger the resistor is the longer the delay time will be. It is recommended to measure delay time with dedicated gate resistor in application. A typical switching time vs. gate resistor value diagram is shown in the following figures:
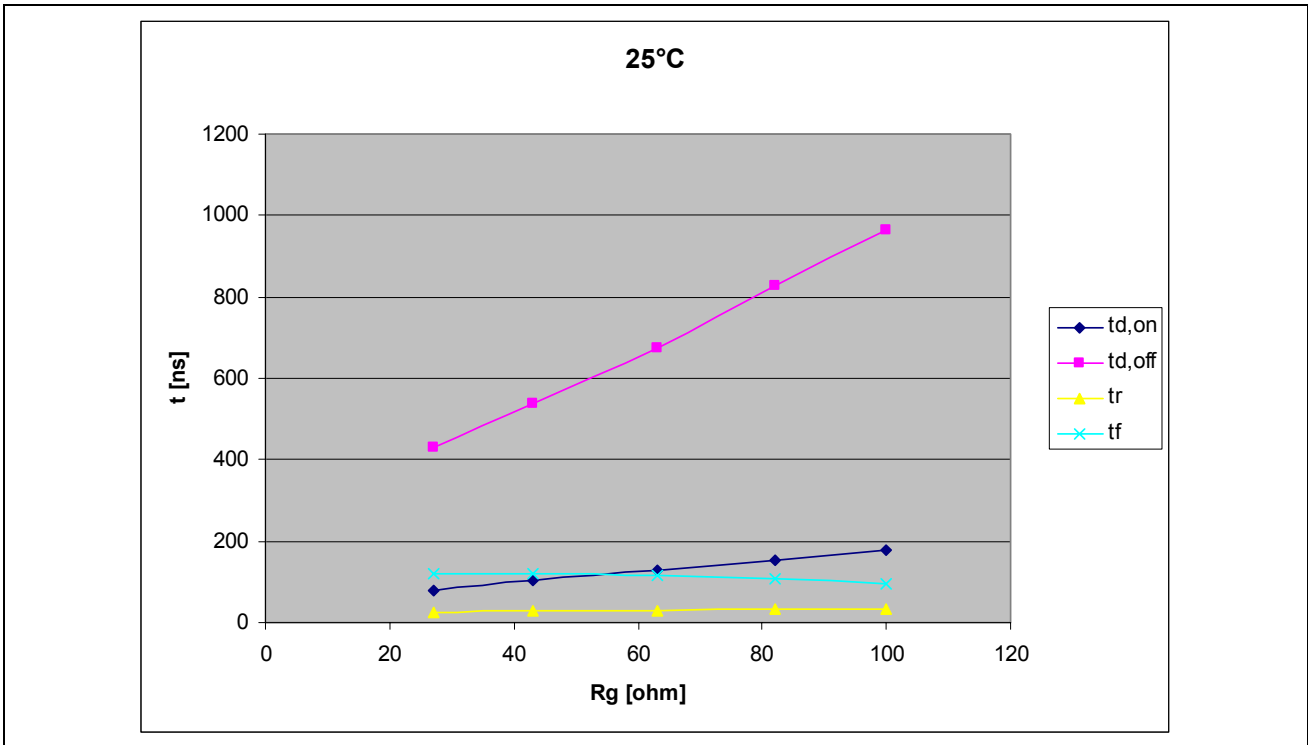

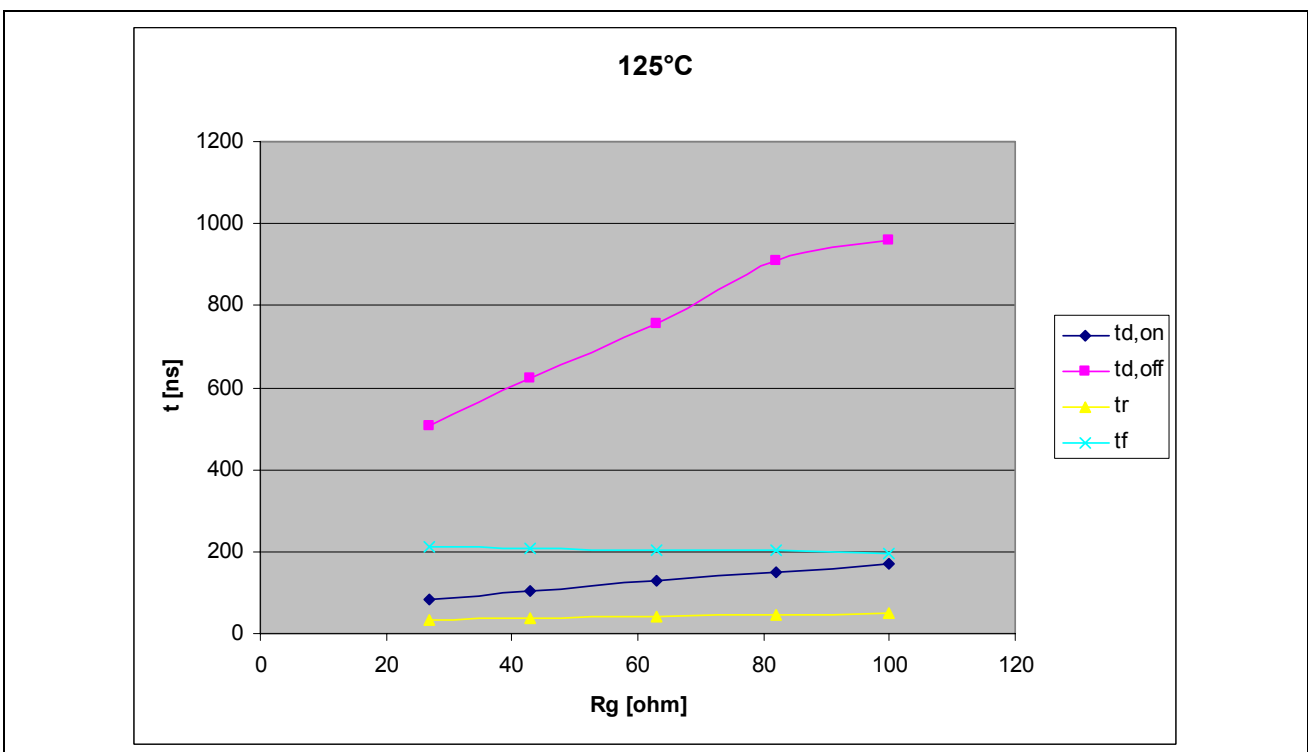
Figure 4 **Switching times vs. Rg @25°C**

Figure 5 **Switching times vs. Rg @125°C**

All tests were done with FP40R12KT3 module, gate voltage is -15V/+15V, DC link voltage is 600V and switched current is nominal current of 40A.

2.4 Impact of other parameters on delay time

Besides the gate resistor values, there are other parameters having significant impact on delay times:

- Collector current.

- Gate drive supply voltage.

2.4.1 Turn on delay time

To estimate this relationship, a series of measurements was done. First the dependence of turn on delay time and current was investigated. The results are shown in the next figure:
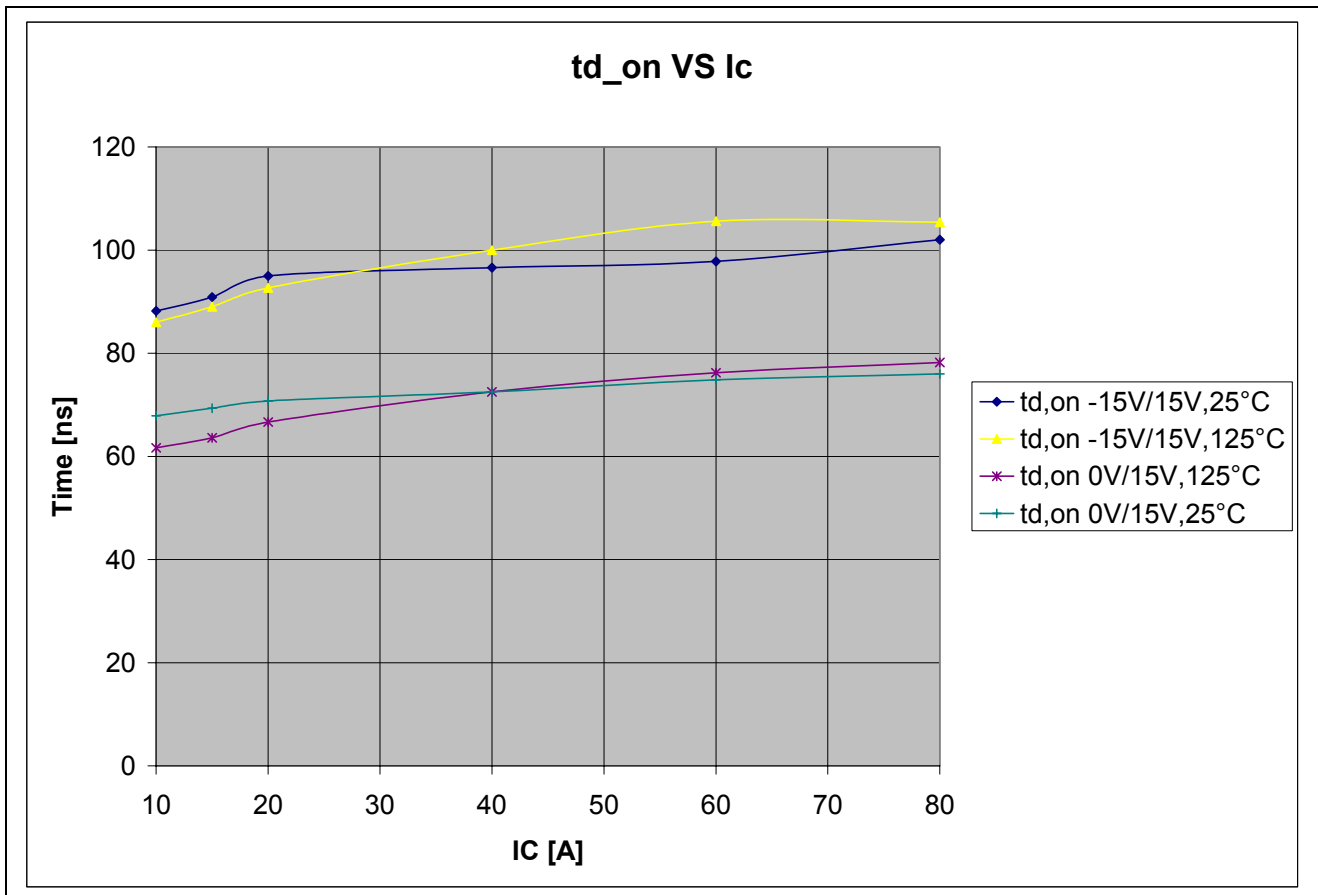

Figure 6   The turn on delay time vs. switched current Ic

All tests were done with a FP40R12KT3 module at a DC link voltage of 600V, gate resistor is chosen according to datasheet value.

From results above it can be seen that turn on delay time is almost constant with variation of collector current Ic. With -15V/+15V gate voltage turn on delay time will get larger than with 0V/+15V gate voltage [2]. For further calculation of control dead time this variation will be neglected since it is quiet small and provides even additional margin.

2.4.2 Turn off delay time

The most important factor in the calculation of dead time is the maximal turn off delay time. Since this value determines almost entirely how long the final calculated dead time will be. So we will investigate this delay time in detail.

In order to obtain the maximum turn off delay time following considerations have to be done:

1. What and how long is the turn on delay time caused by IGBT device itself?

To answer this question the following test based on a characterization driver board is done in laboratory. The characterization driver board is considered as an optimal driver, which means that this particular driver will cause no delay (which is almost true with an oversized driver), so the whole delay time is considered to be caused by the IGBT device itself. Following block diagram shows test setup:
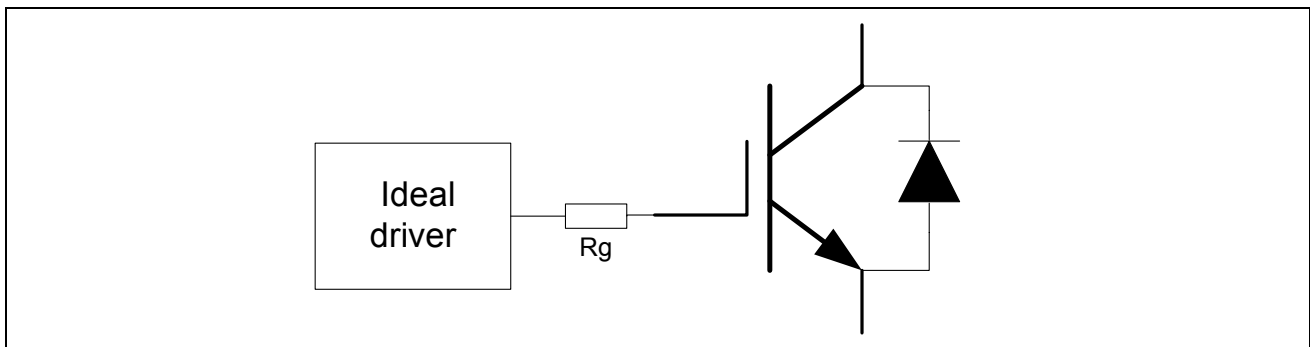

Figure 7   Block diagram of test with ideal driver

2. What is the maximal turn off delay time if the threshold voltage of IGBT has the minimal value in datasheets? (this reflects the tolerance of Vth from module to module)

To answer this question an additional diode is connected to simulate the reduced Vth voltage. The diode has a voltage drop of approximately 0.7…0.8V, which is quite similar to the Vth variation of FP40R12KT3 module. Following block diagram shows principle test setup:
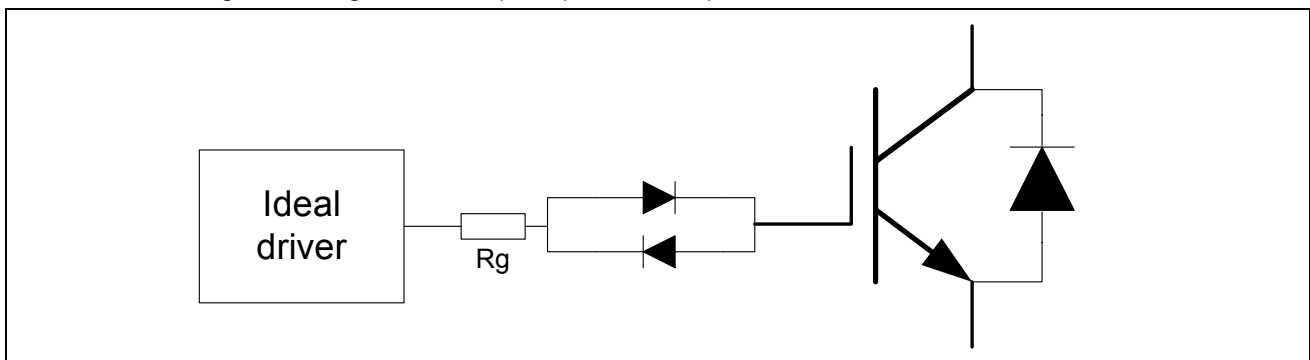

Figure 8   Block diagram of the test to simulate variation of Vth in worst case.

3. What is the impact of driver output stage on switching times?

To answer this concrete question the drivers on the market were splitted into two categories, one with mosfet transistor output stage and the other one with bipolar transistor output stage. For each category separate measurements were made.

To simulate drivers with mosfet output stage, another additional resistor was connected and has been considered as the on state resistor Rds(on) of Mosfet transistor. The diode for simulation of Vth variation remained. The following block diagram shows the principle test setup:
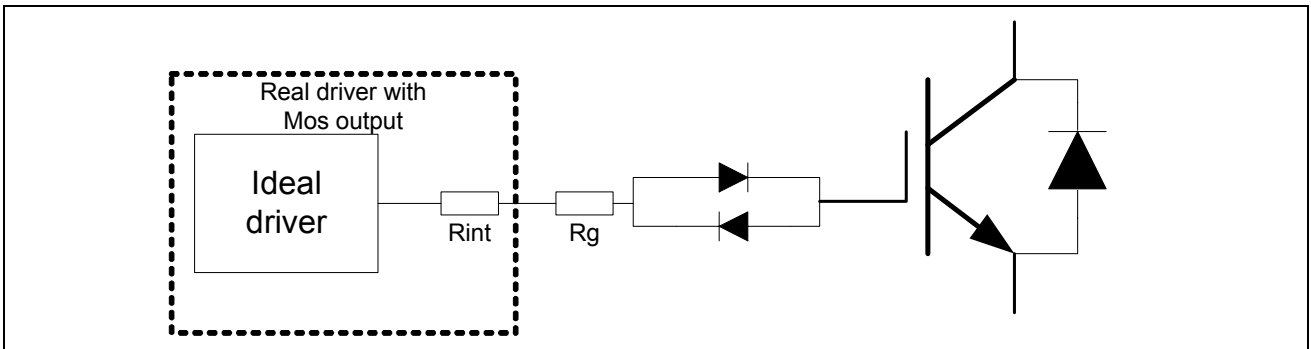
Figure 9   Block diagram of test to simulate variation of Vth and driver with mosfet output.

4. What is the impact of the driver with bipolar transistor output stage?

To answer the question an additional diode which simulated the voltage drop on bipolar transistor within output stage was connected. The following block diagram shows principle test setup:

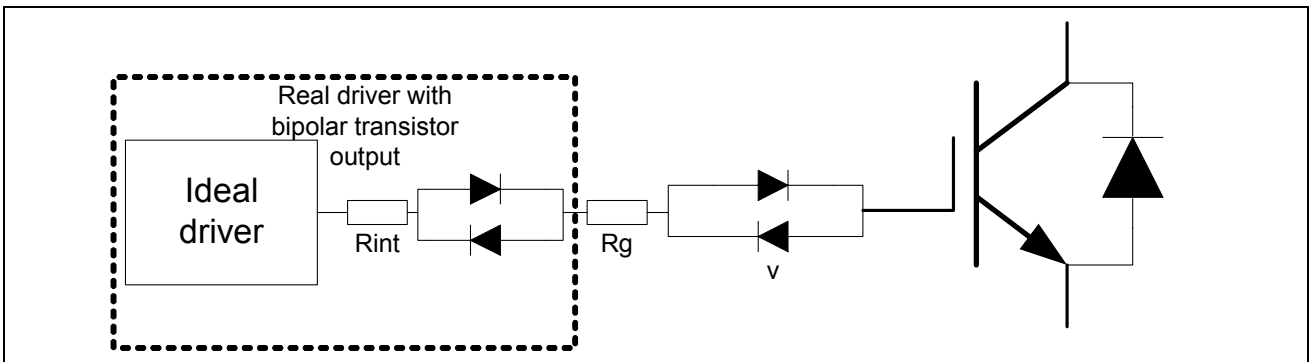**Figure 10   Block diagram of the test to simulate the variation of Vth and driver with bipolar transistor output**

With the configurations shown above the measurement of turn off delay time was done in our laboratory with module FP40R12KT3 and driver board which had been considered as optimal. Test conditions were Vdc=600V, Rg=27Ω. Results are shown in the next two figures:
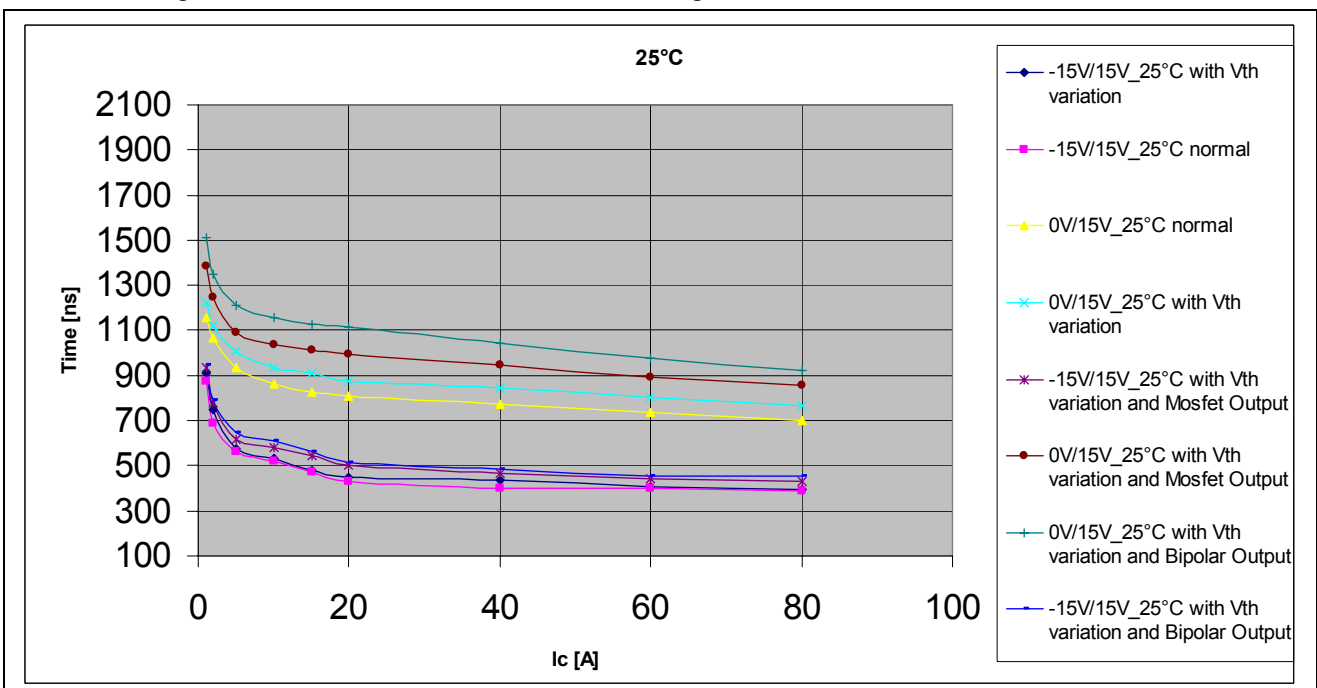

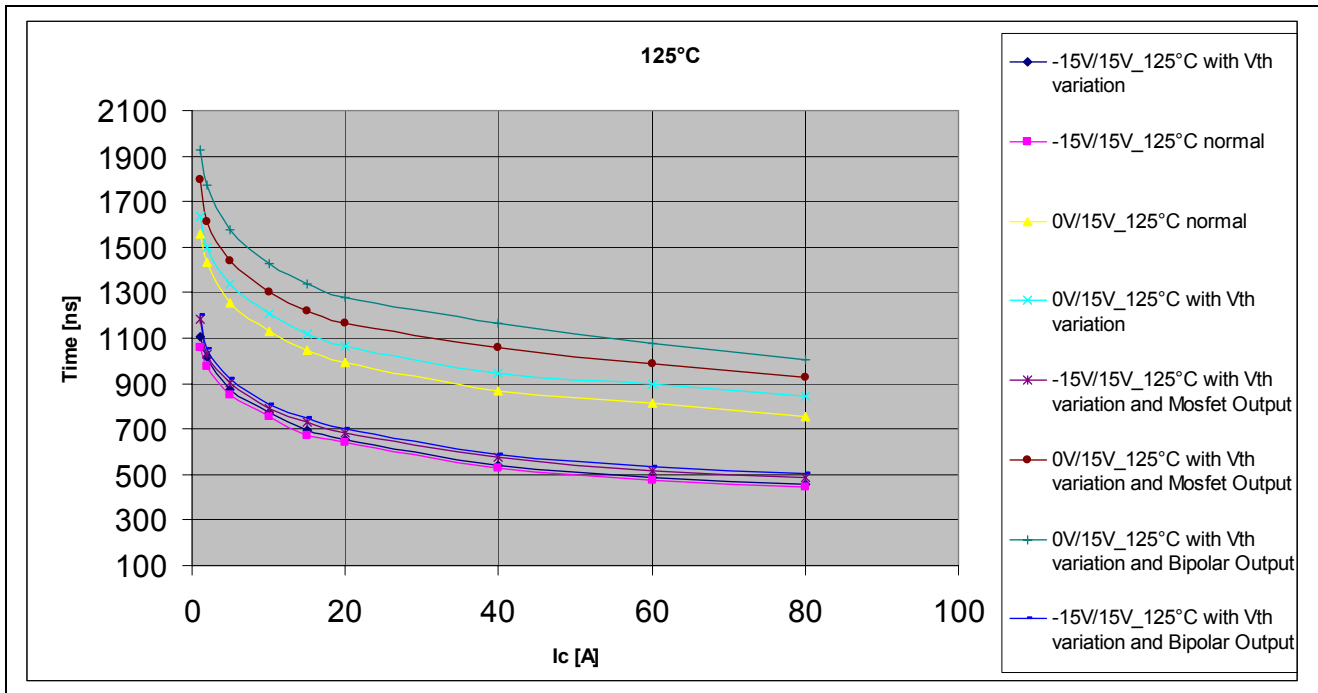**Figure 11   Turn off delay time vs. Ic @25°C**

Figure 12   Turn off delay time vs. Ic @125°C

From the results we can see that there is a significant increase of turn off delay time with decrease of the switched current Ic. So just simply calculate dead time according to a chosen gate resistor is obviously not precise enough. Measuring the delay time under the dedicated driving condition then calculating dead time according to these values is a better and more precise way. Normally measurement until 1% of the nominal current would be enough to give a sufficient overview for calculating required dead time.

Another point to be considered here is that the turn off delay time will increase with 0V/+15V gate drive, and the impact of output stage on switching times will be bigger with 0V/+15V switching. This means that with 0V/+15V switching voltage special care has to be taken by choosing the driver. Additionally, the increase of td_off with lower switched collector current Ic should be considered also.

As an example: the HCPL-3120 driver IC will be considered here. This driver IC has a Mosfet output stage for switching off. From diagrams above we can read the value for td_off under 0V/+15V switching condition is roughly 1500ns. The td_on in this case is about 100ns. The tpdd_max-tpdd_min of this driver IC according to datasheet is 700ns. Applying these values to the formula (1) results in a dead time of about 2.5µs.

2.4.3   Verification of calculated dead time

With the discussion above and the formula (1) given in chapter 2.1 it is now possible to calculate the required dead time based on the measurements above. With the calculated dead time, a worst case measurement can then be performed to verify if the chosen dead time is enough or not.

From the measurement it can be seen that the turn off delay time increases with temperature. From this reason it is preferable that the test should be done both at cold and hot condition.

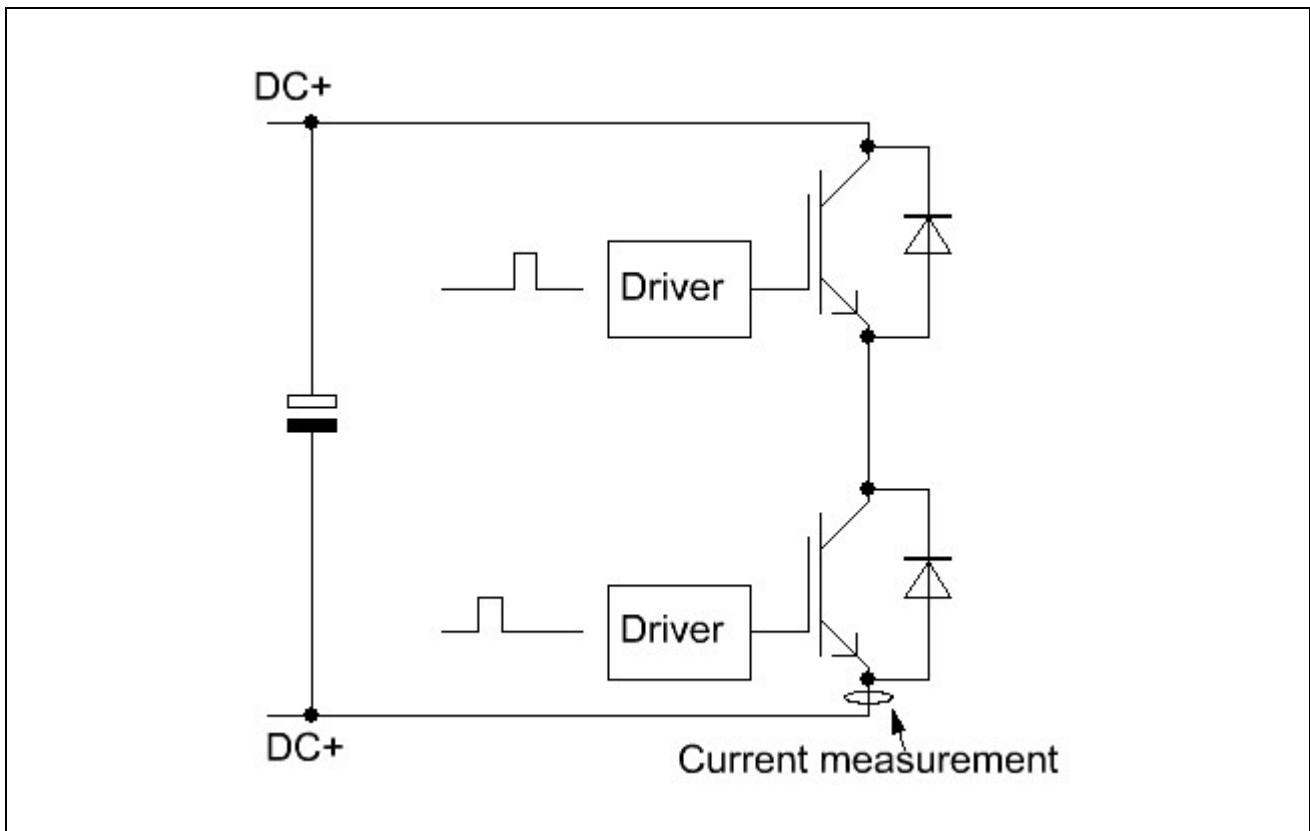The schematic illustration of the test looks like following:

Figure 13   Schematic illustration of test to check calculated dead time value

The bottom IGBT has to be switched on and off, then the same for the top one. The time between the two pulses should be adjusted to be the value of calculated dead time for the dedicated driving condition. The negative dc-link current can then be measured and if the dead time is sufficient, a shoot through current should not be observed.

Since there is no current through both IGBT, the described test represents the worst case condition for dead time calculation. From the discussion of turn off delay time it is known that dead time will be longer with decrease of collector current, so in case there flows no current, turn off delay time should be largest, which leads to a need of largest dead time. If there is no shoot through current at zero collector current then the chosen dead time is for dedicated driving condition sufficient.

3   How to reduce dead time

For a proper calculation of control dead time the dedicated driving condition should be considered:

- What is the applied gate voltage to the IGBT?

- What is the chosen gate resistor value?

- What type of output stage does the driver have?

Based on these conditions a test should be made, from the test results the control dead time can then be calculated using equition (1).

Since dead time has a negative impact on the performance of inverter, it has to be minimized. Several methods can be taken.

- Take a driver strong enough to sink or source the peak IGBT gate current.

- Use negative power supply to accelerate turn off.

- Prefer drivers based on fast signal transmission technology like Coreless Transformer Technology to drivers based on traditional opto-coupler technology.

- If 0V/15V gate drive is used then consider use of separate Rgon/Rgoff resistor as described below.

From measurements shown in chapter 2.3 a very strong dependence of Td_off and gate resistor value can be observed. If the Rgoff reduced then the td_off will be reduced as well as dead time. Infineon suggests reducing the Rgoff to 1/3 of the Rgon value if 0V/15V gate voltage is used. One possible circuit for separate Rgon and Rgoff is as follows:
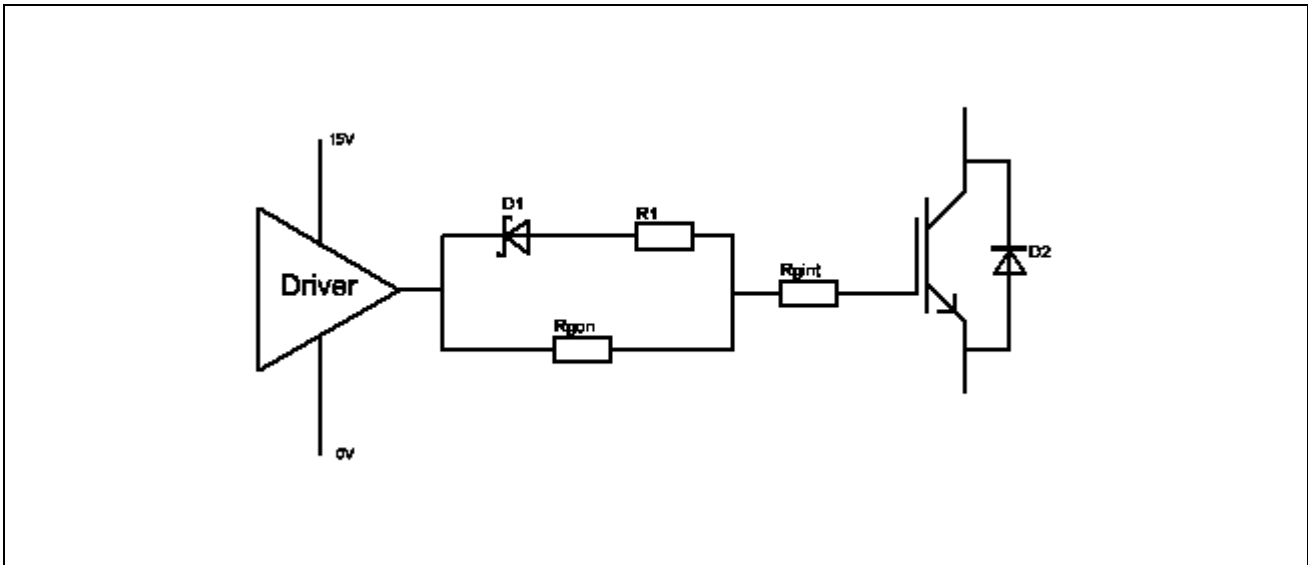

Figure 14   Suggested circuit with 0V/15V gate voltage.

R1 should be chosen to satisfy the following relation:

$$\frac{R_1 \cdot R_{gon}}{R_1 + R_{gon}} + R_{g\,int} = \frac{1}{3} \cdot (R_{gon} + R_{g\,int}) \qquad (2)$$

$$\Rightarrow R_1 = \frac{1}{2} \cdot R_{gon} \cdot \frac{R_{gon} - 2R_{g\,int}}{R_{gon} + R_{g\,int}} \qquad (3)$$

From equation (3) it is to be noticed that the requirement Rgon>2Rgint has to be fulfilled to get a positive value of R1. However, with some modules this requirement can not be true. In this case, R1 can be omitted completely.

The diode should be a schottky type diode.

Another very important issue with 0V/15V gate voltage is the parasitic turn on effect. This issue can be also solved if suggested circuit is used. For more details on parasitic turn on please refer to AN2006-01[2].

4   Conclusion

In this application note an approach of measuring switching times of IGBT and then calculating the control dead time is introduced. First dependence of switching time on gate resistor value was shown, and then influence of gate driver and collector current on switching times was discussed. Finally possible methods to reduce dead time were introduced.

Bibliography

[1]   D.Grahame Holmes, Thomas A. Lipo: „Pulse width modulation for power converters: principles and practice", *IEEE Press, 2003. ISBN 0-471-20814-0*

[2]   Driving IGBTs with unipolar gate voltage.

        http://www.infineon.com/dgdl/an-2006-01_Driving_IGBTs_with_unipolar_gate_voltage.pdf?folderId=db3a304412b407950112b408e8c90004&fileId=db3a304412b407950112b40ed1711291