Thermal performance of surface mount semiconductor packages

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About this document

Scope and purpose

This document analyzes the thermal relationship between the Infineon Surface Mount Device (SMD) packages listed below, via design on the PCB level, and the achievable thermal resistance. The goal of the investigation was to figure out the best combination to keep the packages as cool as possible, while also considering the cost. Reason for an optimal thermal management is that as a rule of thumb a 10°C rise in temperature doubles the failure rate [1].

Table 1 Infineon devices investigated

Packages	Product
PG-VSON-4-1 ThinPAK 8x8	IPL65R230C7
PG-TSON-8-2 ThinPAK 5x6	IPL60R360P6S
PG-DSO-20-85 DSO	IGO60R070D1
PG-HSOF-8-2 TOLL	IPT65R033G7
PG-HSOF-8-2 TOLL	IGT60R070D1

Intended audience

Electronic engineers, dealing with PCBs or other system designs, are the intended audience.

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1 Introduction

The interaction between transistors, package and PCB must be carefully designed to guarantee optimal heat dissipation. The relationship between power dissipation in any component on a PCB and thermal resistance governs the temperature rise shown in Equation 1.

$$Thermal\ resistance\ (R_{th)} = \frac{temperature\ rise}{power\ dissipated}\ [\frac{K}{W}] \quad (1)$$

If the dissipation on a component is 2 W for an R_{th} of 45 K/W the temperature rises by 0 K. Considering an 80 percent derating of the maximum operating junction temperature of 150 K, we get 120 K. This would allow an ambient temperature of 30°C to hit this border. For higher temperatures either the power must be reduced or the thermal resistance must be reduced.

This paper deals with the second two parameters, varying the vias around the different packages. To enable a fair comparison the via matrix under the package was always kept the same.

Chapter 2 explains the thermal dependencies followed by the design parameters, and finally the results and recommendations are shown.

What clearly must be mentioned is that the results are displaying the specific behavior between the chosen transistors and the PCB, varying the vias.

2 Thermal background

2.1 Thermal model

The overall thermal performance of a package soldered to a PCB is characterized by a junction-to-ambient thermal resistance R_{thja}, which can be calculated with the equation shown in Figure 1.

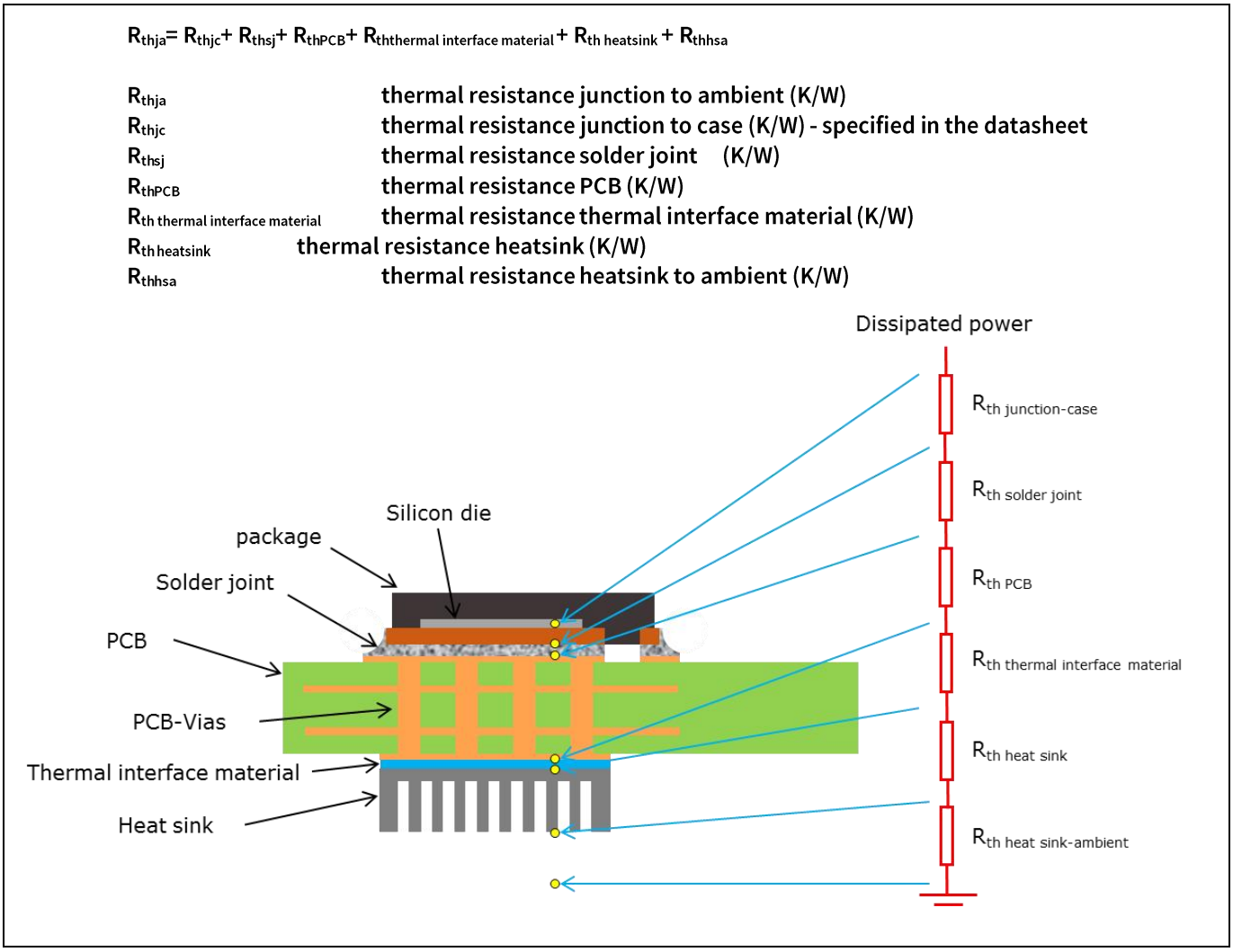


Figure 1 Thermal model of a leadless package soldered to a PCB

Besides the thermal resistance from junction to case, which is specified in the datasheet of the product, the solder joint and the PCB as well as a heatsink (in case it is part of the application design) are contributing factors to the thermal path from junction to ambient.

2.2 Influential parameters in surface mount technology

The most common way to connect an electronic component electrically and thermally to a substrate, usually a PCB, is soldering – or more specifically, surface mount technology. Therefore the solder joint is part of the thermal path from the p/n junction to the ambient. By the nature of the reflow soldering process there will be a certain number of voids in the solder joint, especially on large-area connections you can find below TO packages (DPAK, D^2PAK, TO-leadless), DSO packages and many others. The usual expectation is that voiding in solder joints significantly influences the thermal performance of the soldered package. But this needs to be

considered in much more detail. When looking at the thermal conductivity of the affected materials, a typical value discussed in the field of PCB and application design for lead-free solder (for example SAC305) is ~60 W/mK, whereby the value of the PCB material FR4 is ~0.3 W/mK. This clearly indicates that the influence of the PCB design is much more significant than the voiding rate in the solder joint.

The next step in the thermal path is the PCB. As mentioned above, the thermal conductivity of bare FR4 material is quite poor. Therefore copper features such as thermal through-holes (vias) and additional copper areas for heat-spreading in inner layers of the PCB are necessary for an improved thermal path from component to ambient. Calculating the copper area that is connecting thermally through the board (mainly the cross-section of the copper part of the thermal vias) and reflecting it with the thermal conductivity of the copper material of the PCB (~300 W/mK) will show how to reduce the thermal resistance in the heatsink area. For example 10 percent copper in a heatsink area will lead to a thermal conductivity of ~30 W/mK. The amount of copper in the PCB creating a thermal path through is mainly driven by the number and diameter of the plated through-holes. Also the thickness of the copper features in the different PCB layers needs to be taken into account, as it helps to laterally distribute the heat.

2.3 Influential parameters of the application design

If the PCB is connected to a heatsink or a heat-dissipating part of the housing a thermal interface material is recommended to overcome mechanical tolerances between PCB and heatsink, and also to electrically isolate the heatsink from the circuit.

No matter whether there is a heatsink mounted on the backside of the PCB or if the board is connected to a heat-dissipation feature in the housing, this changes the properties of the overall heat-path. If the sum of all the R_{th} values described in Figure 1 is quite low, the single portions of the heat-path become more important for the whole system. If the overall R_{th} to ambient is much higher than most of the single portions, you can only improve the thermal performance by decreasing the most prominent single R_{th}. For example, if no heatsink is mounted on the backside of the PCB the thermal resistance between PCB and ambient will be the dominant bottleneck for heat transfer, whereby voiding in solder joints is not the main contributor to the overall thermal resistance.

3 PCB design parameters

3.1 THT vias

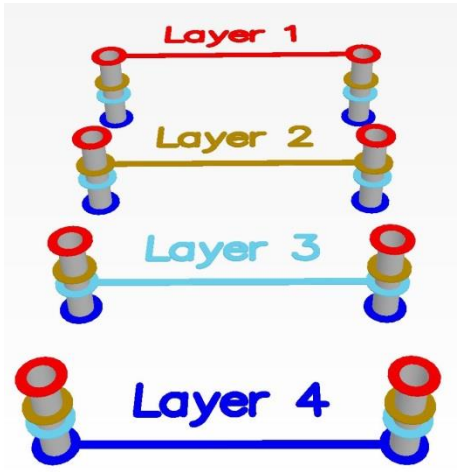


Figure 2 THT vias

Figure 2 shows THT vias for a four-layer PCB. What must be considered in the design is the aspect ratio, which is the relationship between hole diameter and thickness of the PCB. This directly influences the copper thickness within a via, which is normally around 25 µm. In the context of heat management a via represents a thermal resistance from top to bottom. Detailed design constraints must be discussed with the PCB vendor.

3.2 Via matrix

As explained in the previous chapter, vias represent thermal resistances through PCBs. We can lower this resistance significantly by creating a matrix with several vias. The R_{th} calculation follows simple parallel resistors.

3.3 Heat-spreading in the PCB copper layer

To find out the effects of heat-spreading by increasing the copper areas in the PCB Infineon did R_{thja} measurements on different PCB designs, using the same solderable area for all options but increasing the copper area below the solder mask and in the inner PCB layers. Basically it should be pointed out that the results are product specific and will vary if a different product or package is used. What can be taken from the results is the general trend between different layouts and via designs.

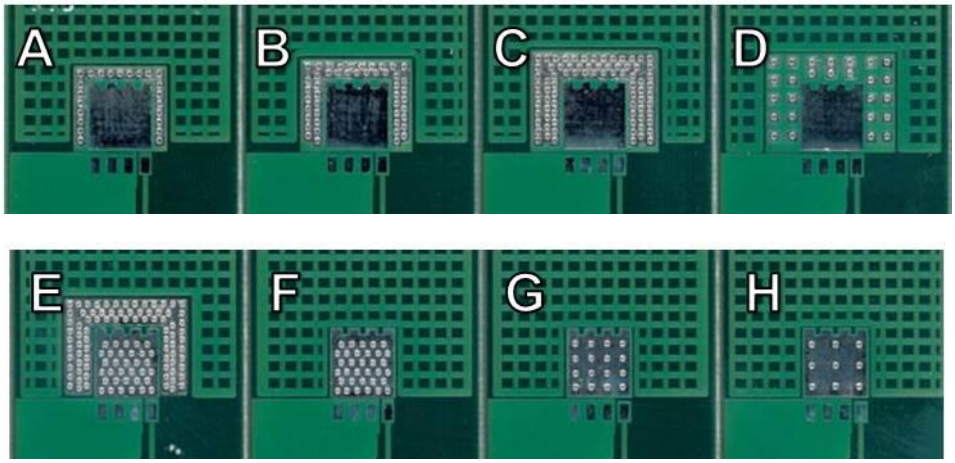


Figure 3 Different layouts for R_{th} measurements on heat-spreading effects

Figure 3 shows eight different layouts for the same package (PG-TDSON-8), which vary in number and location of thermal vias in the PCB. The examples A to D have different numbers of vias distributed around the footprint, while layouts F to H only have vias in the die pad of the footprint. Layout F is a combination of both.

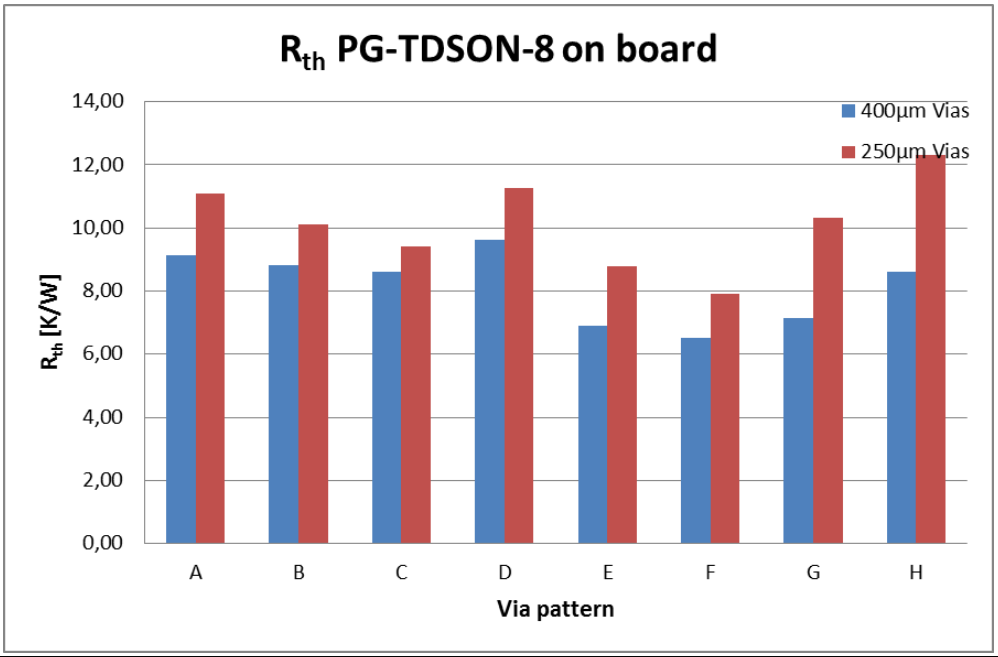


Figure 4 R_{th} measurements on a certain product in an Infineon PG-TDSON-8 package

Looking at Figure 4, a few conclusions can be drawn. Comparing the R_{th} values of layouts A to D, they only vary by about 10 percent. This means if there are vias only distributed around the footprint, a different number of vias does not have a big influence on the thermal resistance. The biggest effect is seen if vias are distributed below the package die pad, which means they are exactly below the heat source, i.e. layout D vs layout F. Additionally the number of vias below the package has some influence on the thermal resistance – see layouts F, G and H. More vias leads to a reduced thermal resistance.

A last observation from Figure 4 is the fact that bigger vias, which means more copper content in the PCB, leads to lower R_{th} values (compare the blue and the red bar of a particular layout).

3.4 Influence of the solder joint

3.4.1 Voids in solder joints

Given the nature of the process and the materials which need to be used, soldering in a classic reflow process – using for example forced convection, the appearance of voids in solder joints, especially for land grid array packages or packages having a large die pad on the bottom side, is unavoidable. Since there are lots of different influencing factors on the appearance and number of voids in a solder joint, there's no general formula for how to get rid of them. A few things to be considered when trying to reduce voiding are mentioned in the following paragraphs. However, before spending lots of effort on voiding it should be considered how significant their influence on the thermal path of the system really is.

Simulations have been performed by Infineon to show the influence of voiding in solder joints on the R_{th} junction ambient. As already mentioned, the R_{th} of the solder joint is important because it can be a significant contributor to the overall thermal resistance of the system. For the simulations described below the ambient temperature was set to a fixed value, which means the thermal transfer from PCB to ambient is very good. Figure 5 describes the result of a simulation for two different lead-frame thicknesses, which represent different package technologies; 1.27 mm is typically in use in TO packages, 0.5 mm in TO leadless. The graph shows that the R_{th} will rise by less than 10 percent when 50 percent of the heatsink solder joint is lost due to voiding. The difference in the two lead-frame thicknesses represents the vertical heat distribution in the package. The base for the simulation has been a four-layer PCB stack-up with a matrix of 15 × 15 thermal vias in the heatsink area.

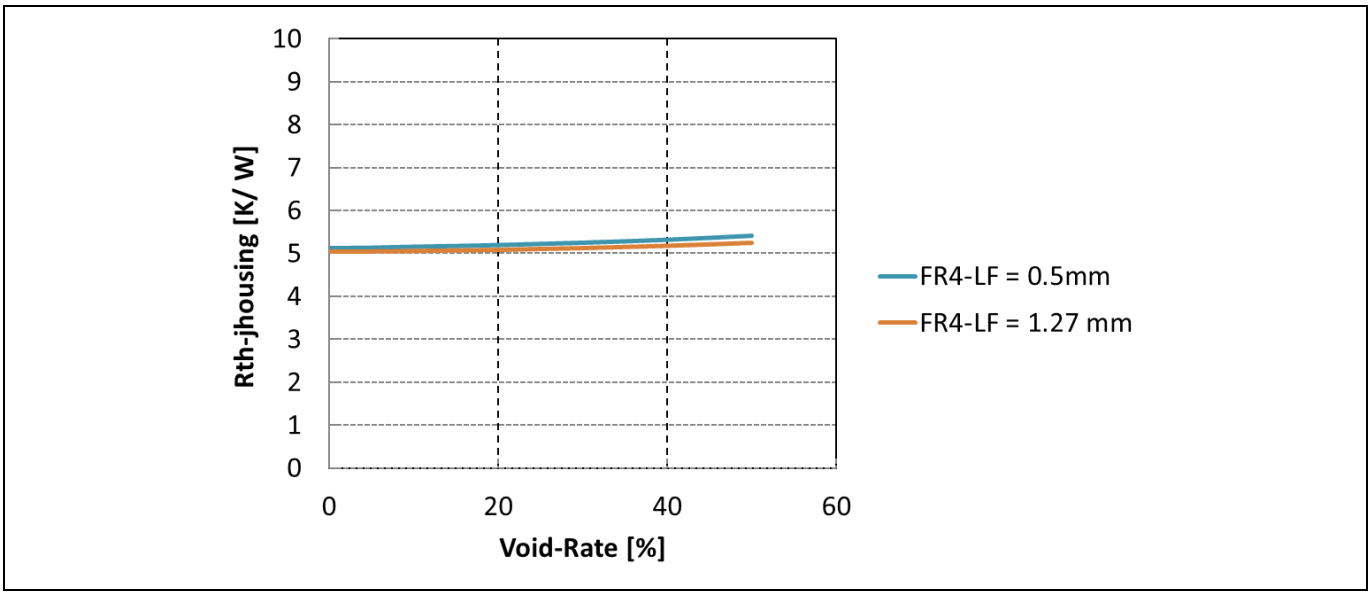


Figure 5 Influence of the solder joint voiding rate on the thermal resistance for TO/TO-leadless packages soldered on FR4, dependent on the thickness of the package lead-frame

Additionally Infineon performed simulations on the influence of solder voids on the dynamic thermal resistance of certain products. Figure 5 shows the design of the PG-TDSON-8 package considered in the simulations, and an example of the void distribution in the solder joint right underneath the silicon die. The package contains a lead-frame of 250 µm thickness and a die size of 2 mm^2. The voiding level has been varied from 0 percent of the die pad area ("perfect solder joint") up to 80 percent ("severe voiding level"), shown in Figure 7 . The PCB below the package was considered to have four layers including a matrix of thermal vias (through-holes) below the die pad solder joint.

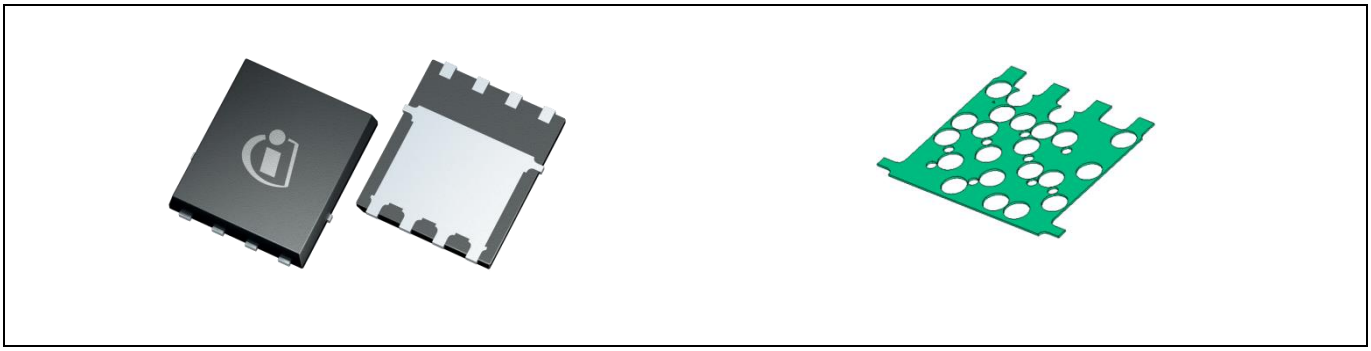


Figure 6 Infineon PG-TDSON-8 package (left) beside an example of voids in the solder joint (right) used during simulation

Figure 7 shows the result of this thermal simulation. For solder joints of up to 30 percent of the die pad solder joint area the dynamic thermal resistance (Z_{th}) is only reduced by 3 percent for short pulsed signals in the range of 10 ms.

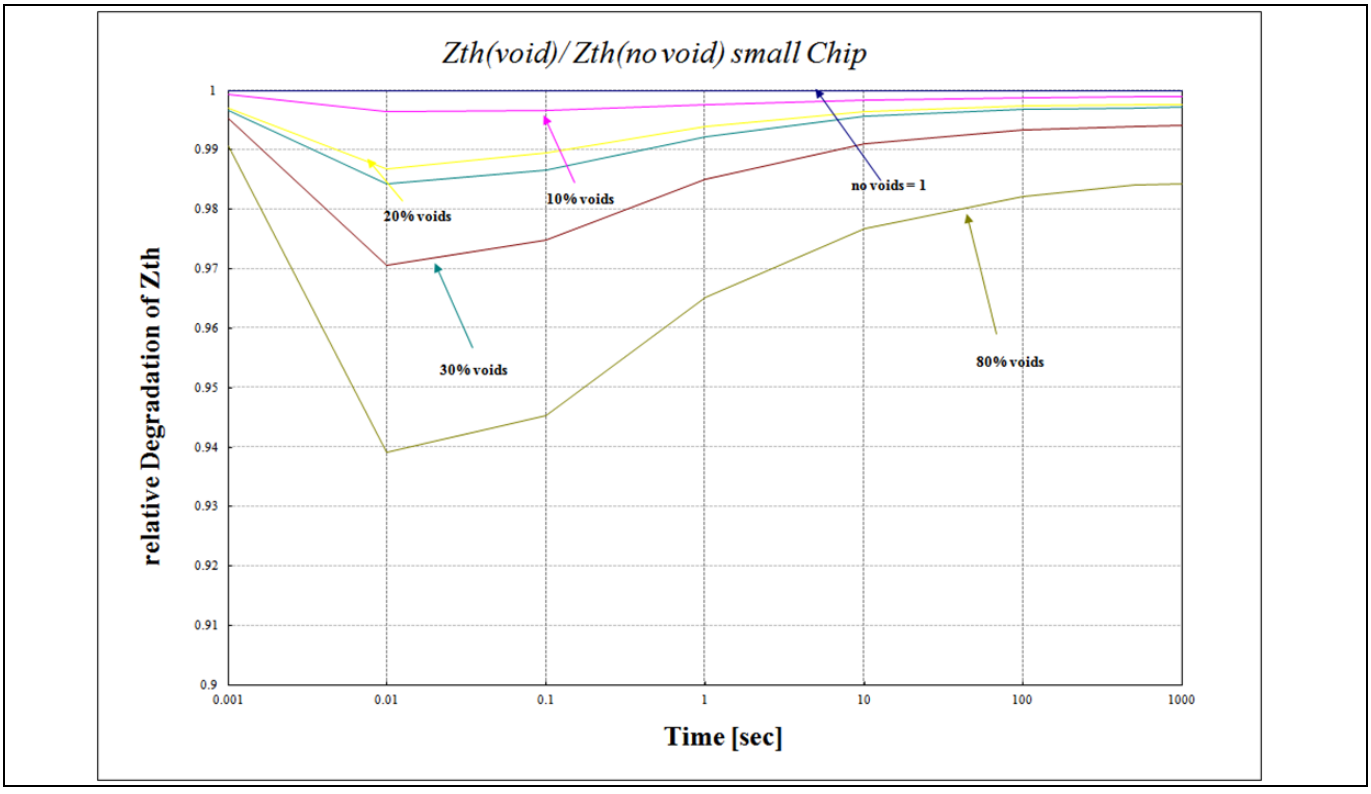


Figure 7 Relative degradation of the $Z_{th(ja)}$ compared to a void-free solder joint for small chips in a PG-TDSON-8 package

One possibility to improve the overall thermal resistance is to use Insulated Metal Substrate (IMS) instead of FR4 PCBs. The specific thermal resistance value depends on the insulation layer used on top of the metal base material (aluminum in most cases) but this is likely better than FR4 PCB material including thermal vias. As mentioned above, the lower the overall thermal resistance, the more interesting are the single R_{th} values such as the effect of voids in a solder joint. For example Infineon did an equal thermal simulation (Figure 4) but using IMS instead of FR4 with thermal vias. In Figure 8 you can see that a void rate of 50 percent raises the R_{th} by 20 to 25 percent depending on the thickness of the lead-frame. In such cases it might make sense to have a closer look at solder joint voiding levels and how they can be improved.

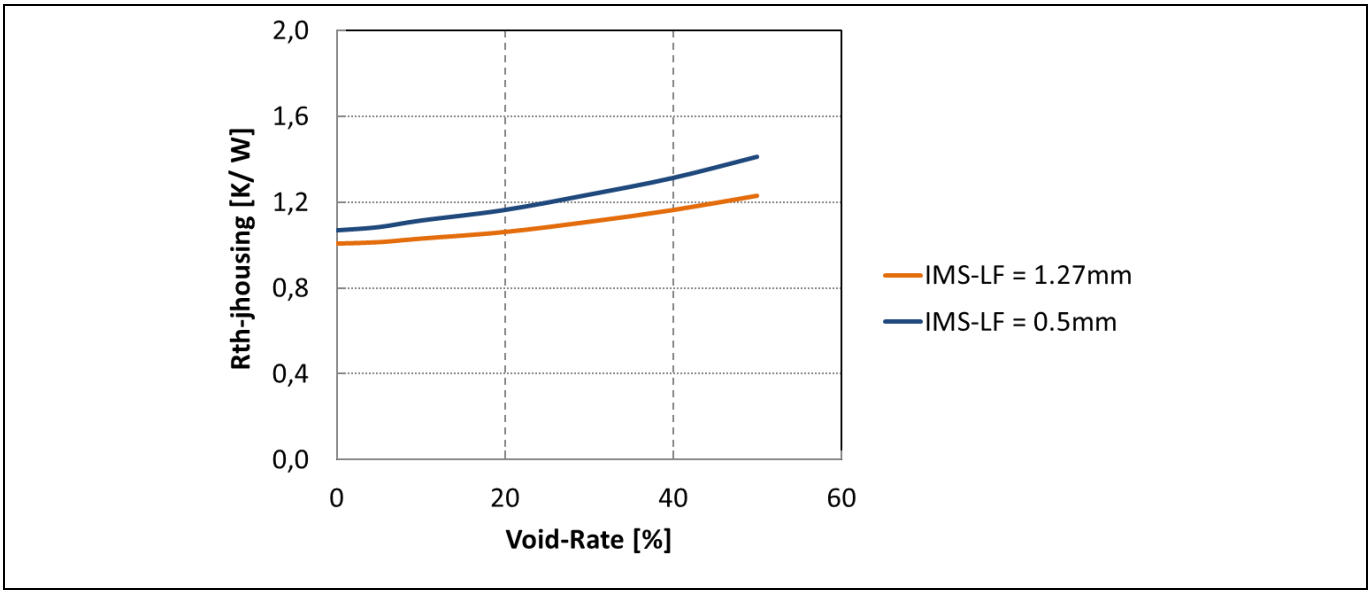


Figure 8 Influence of the solder joint voiding rate on the thermal resistance for TO/TO-leadless packages soldered on IMS, dependent on the thickness of the package lead-frame

In summary, it can be concluded that voids have very little influence on the thermal behavior of FR4 PCBs. IMS must be analyzed separately. Figure 7 shows that for short time pulses, e.g. line-cycle drop-out, voids do have an influence, but this can defined as minor.

3.4.2 Footprint and stencil design

When talking about footprint design there are two main categories: solder-mask defined and non-solder-mask defined footprints.

Solder-mask defined pads

If the metal pad is larger than the solder mask opening, its extensions are solder-mask defined (Figure 9). The definition of solder pads by masking on the metallization allows for wider conductor lines that are especially benefical for devices that are exposed to high currents.

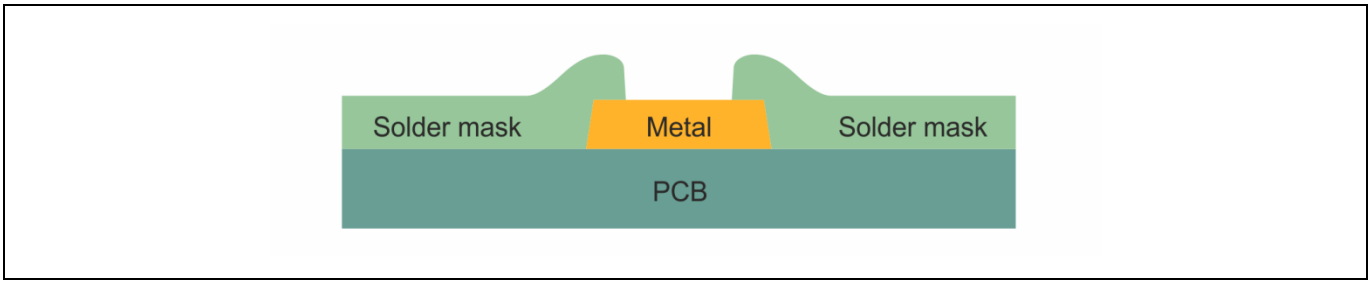


Figure 9 Solder-mask defined pad

Non-solder-mask defined pads

In non-solder-mask defined pads, the metal pad is surrounded by a solder-mask clearance (Figure 10). Dimensions and tolerances of the solder-mask clearance have to be specified to ensure that the mask does not overlap the solder pad. Depending on the PCB manufacturer's tolerances, 50 µm to 75 µm are widely used clearance values.

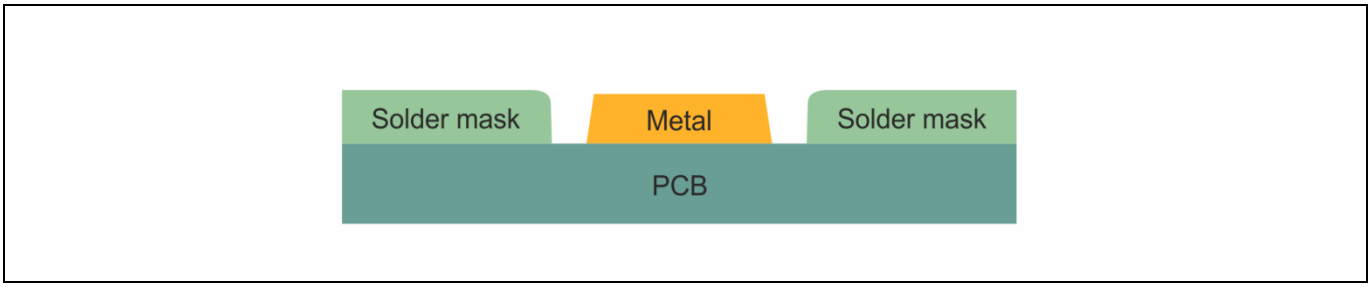


Figure 10 Non-solder-mask defined pad

In terms of thermal performance there are advantages to solder-mask defined footprints because they can be connected to large copper areas on the PCB. This might provide the opportunity of putting more thermal vias underneath or next to a component, which provides an improved heat transfer. On the other hand, solder-mask defined footprints are defined by small side-walls of solder mask on top of the copper structure. These walls tend to prevent some air and gases escaping from the solder joint during the reflow process. Besides this disadvantage the positive aspects of thermally advanced footprints, especially the possibility of improved heat spreading and additional space for vias, lead to the conclusion that solder-mask defined footprints are the design of choice.

When it comes to the stencil design used to apply solder paste to the PCB it is necessary to find the right design depending on different requirements, the need to reduce the amount of solder paste for large-area solder joints (x- or y-dimension greater than 5.0 mm) as well as the alignment with the footprint dimensions, e.g. respecting solder-resist tolerances by a small size reduction for solder-mask defined footprints. Additionally the stencil openings for large-area solder joints should be separated in a matrix of single openings. Such designs are said to enable more gases produced by the contents of flux to escape through the channels provided by the printing design. This is illustrated in Figure 11. The width of the channels is typically 0.4 mm or larger.

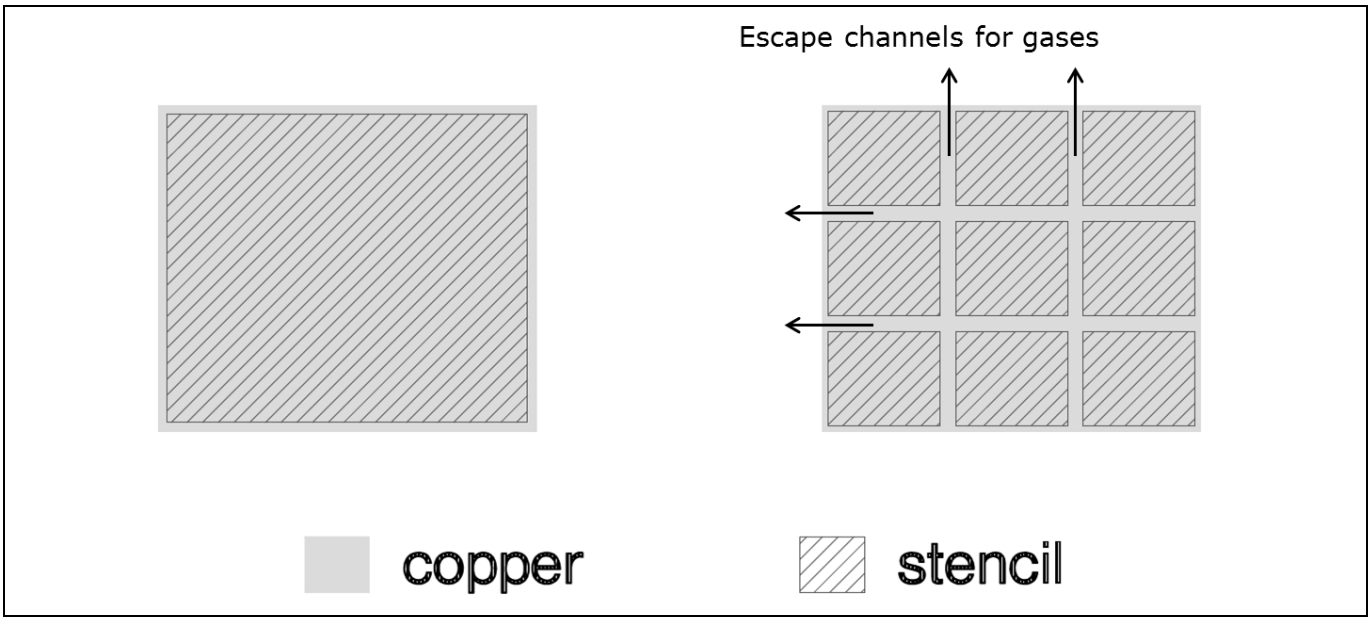


Figure 11 Comparison of stencil designs for large-area solder joints – one single opening vs a matrix of smaller openings to provide channels for gas to escape

3.4.3 Reflow soldering technology

If the overall thermal design of the application requires an optimized thermal resistance of the solder joint (e.g. in case of an IMS and a very good thermal path through a heatsink) it is necessary to take a close look at the solder paste used. The void-responsible part of the solder paste is the organic content, typically flux and solvents. The composition of the organic part differs between solder paste manufacturers, and even a single company usually offers more than just one type of flux. Ask the solder paste manufacturer for advice on using the right solder paste for soldering applications which are susceptible to solder joint voiding. Additionally the dedicated recommendations for the paste in use regarding the reflow profile should be taken into account.

Reflow soldering profiles can be divided into separate phases, as shown in Figure 10. Very generally, the most critical part for voiding is the soaking. In this area a solder paste optimized for temperature and time has to be developed on the respective application to achieve the lowest possible voiding rate in standard convection reflow equipment.

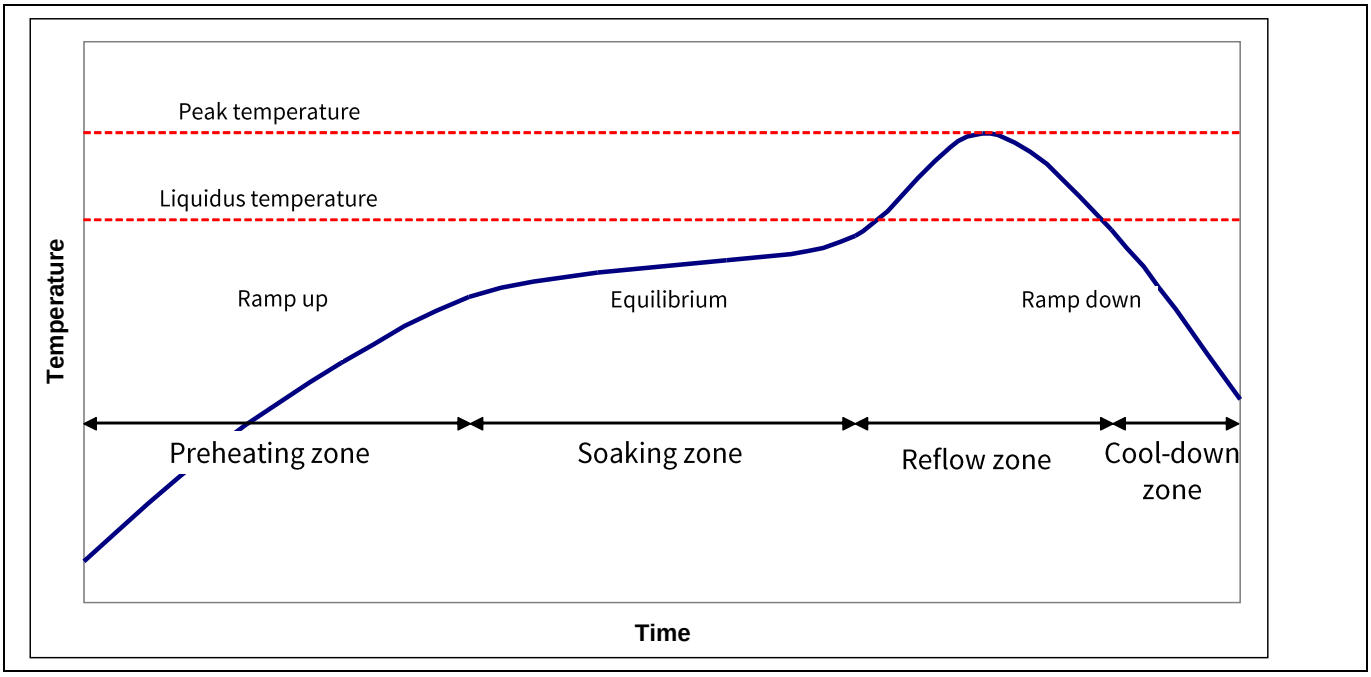


Figure 12 Different sections of a temperature profile used for reflow soldering

If the required voiding level cannot be achieved by the temperature profile adaptations described, an additional way of significantly reducing voids is soldering in a vacuum. Several vendors of reflow equipment offer vacuum solutions for convection soldering as well as condensation soldering.

Convection soldering in a vacuum usually works in a similar way to the standard reflow. The main difference is an extended peak time due to the fact that a vacuum needs to be present while the solder is in a liquid state.

Condensation soldering uses the heat transfer by the condensation of a special liquid on the electronic assembly. This leads to a homogenous heating of the assembly. Due to the different heating temperature profile condensation soldering does not offer a long soaking zone, but heats up the assembly in a much more linear way. Therefore it is recommended to use a vacuum option for condensation soldering. Figure 11 shows the different voiding levels achieved when using condensation soldering with and without a vacuum. In general, equipment vendors promote their machines as being able to produce voiding rates in a low single-digit percentage range.

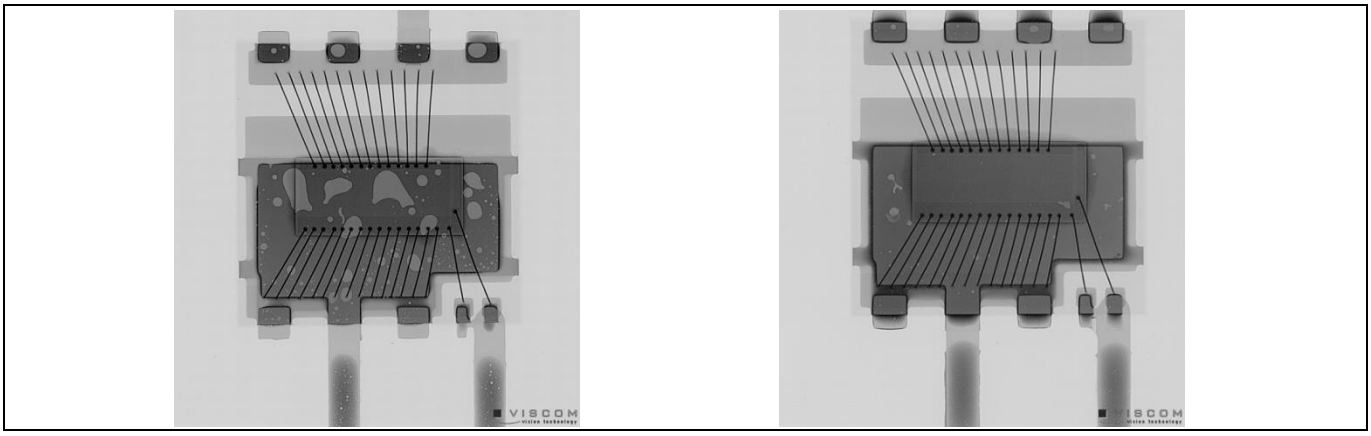


Figure 13 **X-ray images of solder joints created by convection (left) and condensation with vacuum (right)**

4 Measurement set-up

To achieve reliable results the following set-up was chosen:

The single PCBs were fixed with two mechanical quick releases to guarantee a uniform and reproducible pressure. As Thermal Interface Material (TIM) the Bergquist Sil-Pad® K-10 with an R_{th} of 2.01 K/W at 50 psi was chosen.

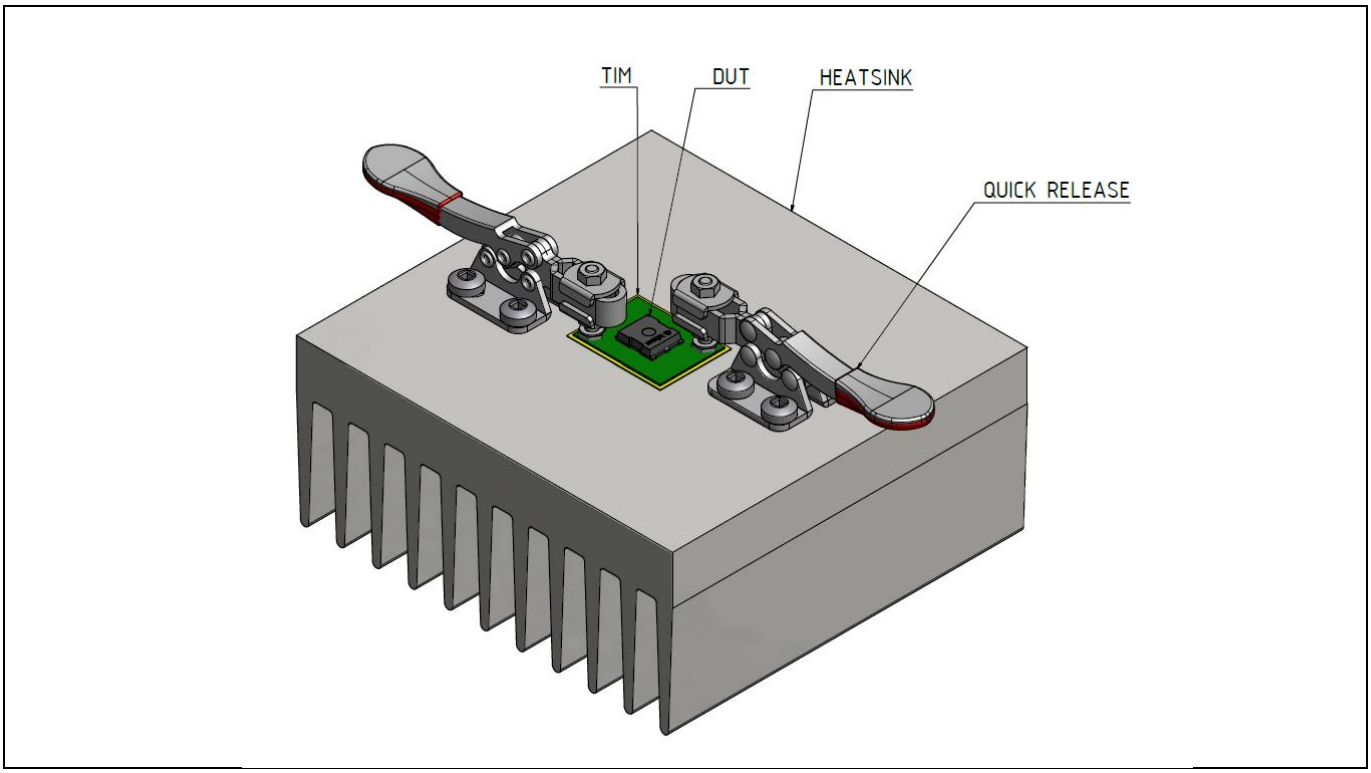


Figure 14 Mechanical set-up

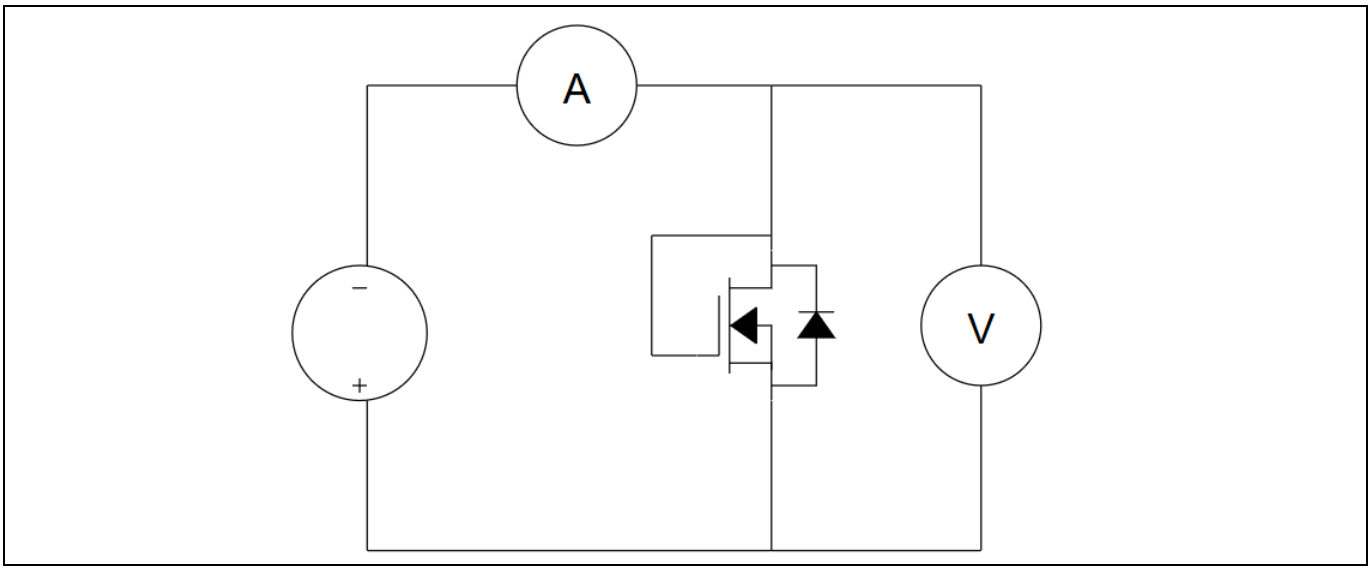


Figure 15 Measurement schematic

The simplified relationship between dissipated power and temperature rise is as follows:

Measurement set-up

$$Thermal\ resistance\ R_{(th)} = \frac{temperature\ rise}{power\ dissipated}\ [\frac{K}{W}] \quad (1)$$

The measurement was done in that way; a certain current was applied on the body diode. The diode voltage was measured and the power calculated from that.

The temperature was sensed on the heatsink close to the DUT and on the mold compound of the package with a thermal camera.

Measurement example:

Applied current: 1 A Measured voltage: 0.7 V Resulting power: 0.7 W

Temp. of heatsink: 24°C Temp. of DUT: 34°C ΔT = 10°C

$$Thermal\ resistance\ R_{(th)} = \frac{10}{0,7} = 14,28\ [\frac{K}{W}] \quad (2)$$

Table 2 Measured devices

Package	Product	Measurement numbers
PG-VSON-4-1 ThinPAK 8x8 	IPL65R230C7	120
PG-TSON-8-2 ThinPAK 5x6 	IPL60R360P6S	144
PG-DSO-20-85 DSO 	IGO60R070D1	144
PG-HSOF-8-2 TOLL 	IPT65R033G7	144
PG-HSOF-8-2 TOLL 	IGT60R070D1	144
	Total	696

Table 2 should enhance the statistical significance of the measurements.

5 Results and interpretation

In the following chapter the results are presented by first showing the PCB structure, then the associated via matrix table, followed by the graphical representation of the results. As a basic reference via Variant 1 is always shown in the graphs. The via diameter was 0.3 mm.

5.1 ThinPAK 8x8

Figure 16 shows the applied matrices in the different variants and the covered areas.

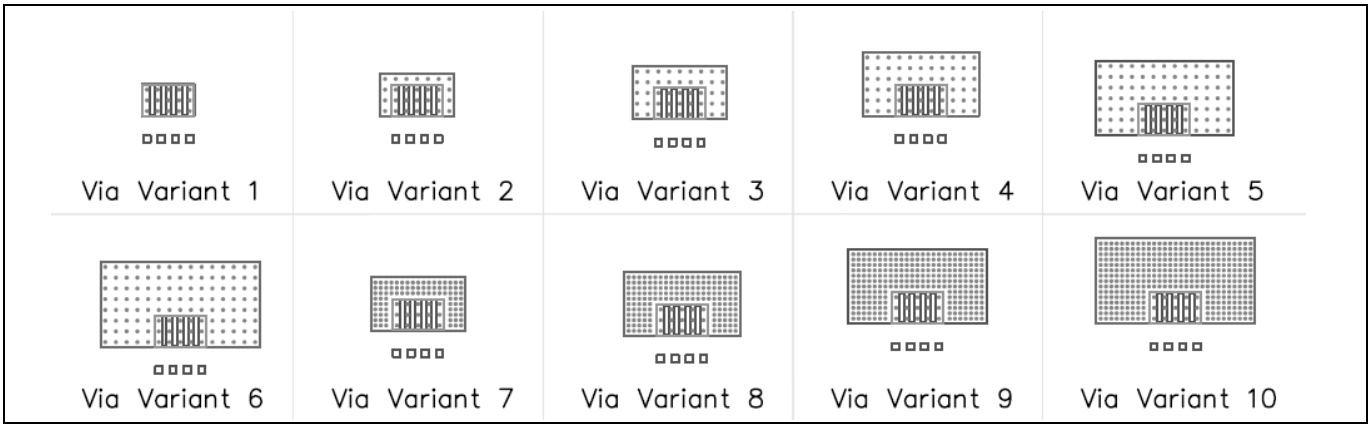


Figure 16 PCB structure ThinPAK 8x8

Table 3 shows the specifications of the matrices and the necessary areas in absolute and relative numbers. One additional presented parameter is the covered area for the different variants and the relationship as a percentage. This means that Variant 1 needs 31.7 mm^2 and Variant 10 266.5 mm^2, which is 636 percent more area covered. This structure of analysis is applied to all packages.

Table 3 ThinPAK 8x8 matrices and covered area

Via variants	1	2	3	4	5	6	7	8	9	10
Via inner	3 × 5	3 × 5	3 × 5	3 × 5	3 × 5	3 × 5	3 × 5	3 × 5	3 × 5	3 × 5
Via pitch inner	1.5 mm	1.5 mm	1.5 mm	1.5 mm	1.5 mm	1.5 mm	1.5 mm	1.5 mm	1.5 mm	1.5 mm
Via matrix outer	3 × 5	4 × 7	5 × 9	6 × 11	7 × 13	8 × 15	9 × 17	11 × 21	13 × 25	15 × 29
Via pitch outer	1.5 mm	1.5 mm	1.5 mm	1.5 mm	1.5 mm	1.5 mm	0.75 mm	0.75 mm	0.75 mm	0.75 mm
Covered area (mm^2)	31.7	61.3	99.1	145.9	201.7	266.5	99.1	145.9	201.7	266.5
Covered area (percentage)	100	193	313	460	636	841	313	460	460	636

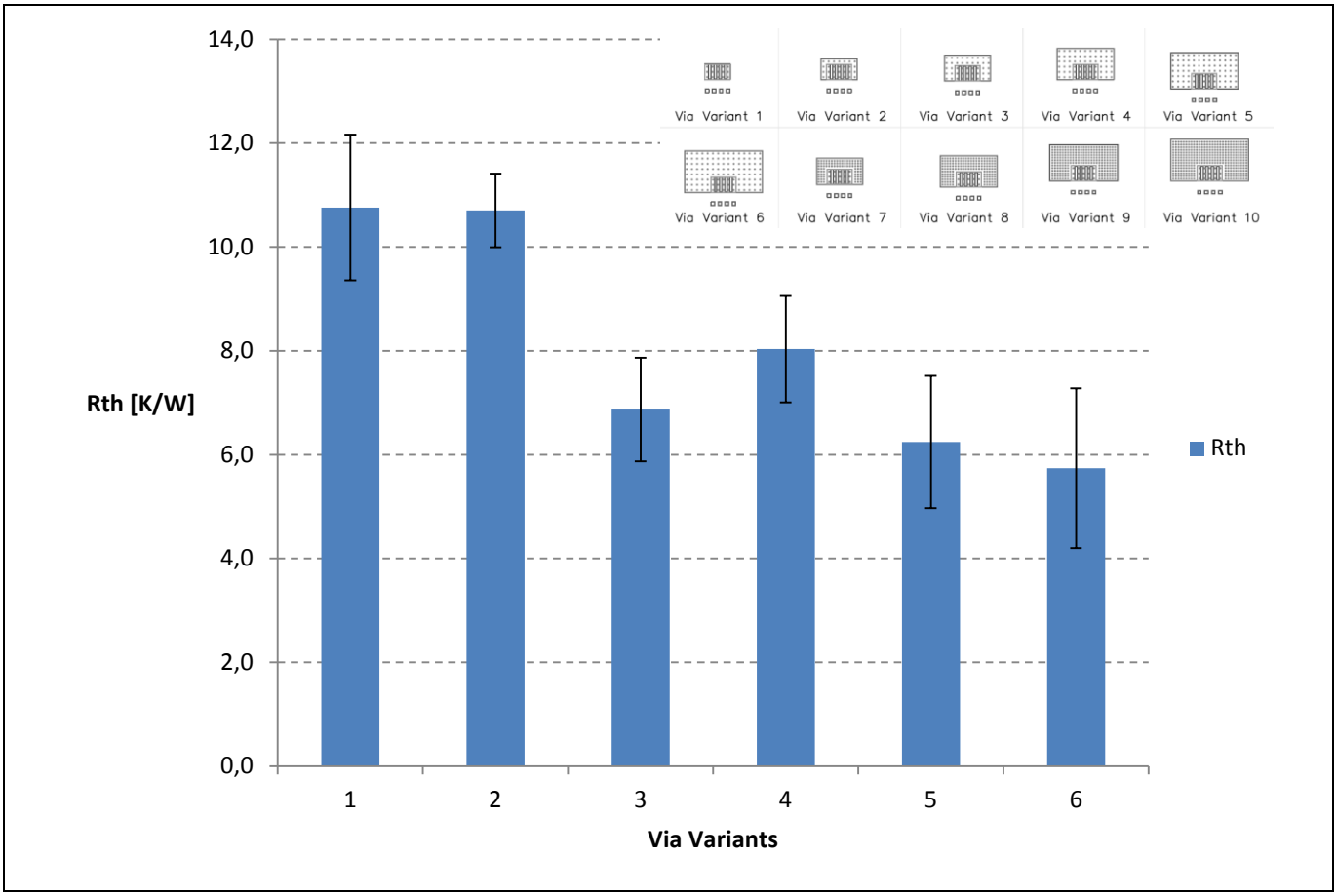


Figure 17 ThinPAK 8x8 V1 to V6 results

Figure 17 shows that the R_{th} can be reduced from Variant 1 to Variant 6 by around 48 percent (10.8 to 5.7 K/W). If the covered area is further increased a saturation can be expected.

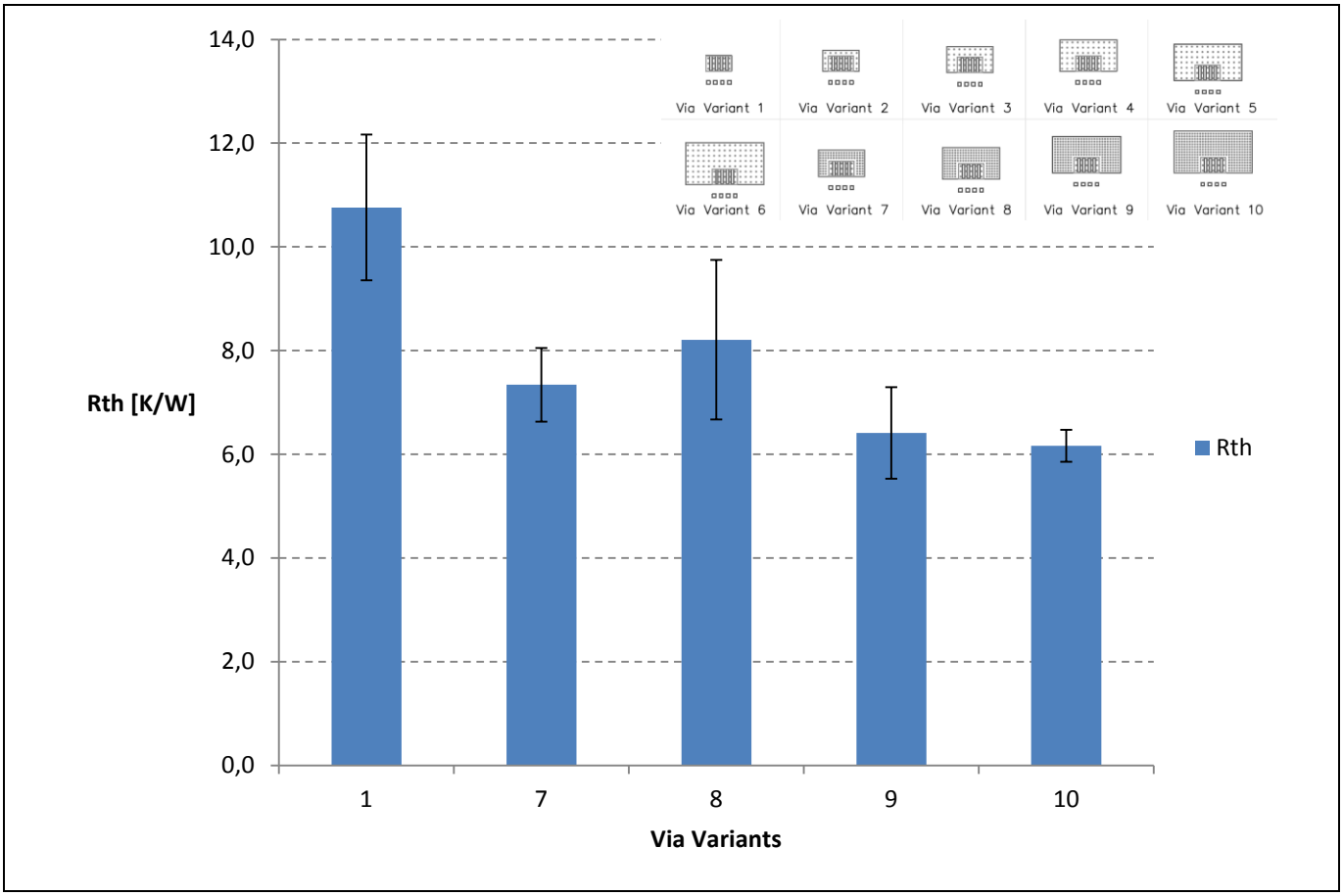


Figure 18 ThinPAK 8x8 V1, and V7 to V10 results

The usage of a higher via density has no better effect in comparison to Variants 1 to 6, as can be seen in Figure 18. The lowest R_{th} value is 0.5 K/W higher, as the lowest visible in Figure 17. The standard deviation is in both cases in a range of 2 K/W.

As result we recommend using the less dense approach to achieve the best performance in relation to cost. This is represented in Variant 5 or 6. The difference between this and other variants is the covered area presented in Table 3.

This recommendation was applied on the telecom demo board 1400 W phase-shifted full-bridge with CFD7 in ThinPAK.

https://www.infineon.com/cms/en/tools/solution-finder/product-finder/evaluation-board/

5.2 ThinPAK 5x6

Figure 19 shows the matrices used and the covered areas for the different variants.

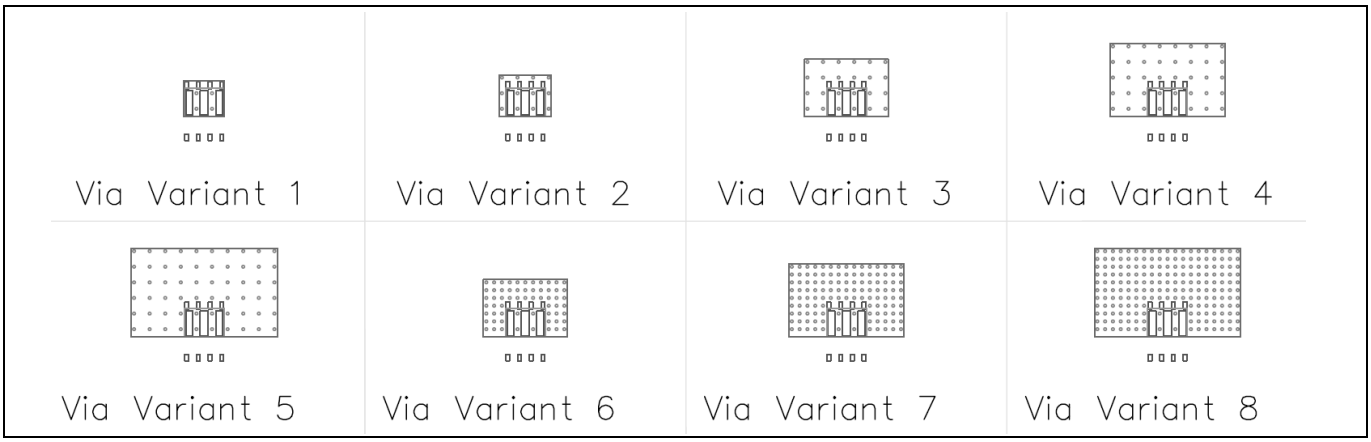


Figure 19 PCB structure ThinPAK 5x6

Table 4 shows the matrices used and the covered areas in absolute and relative numbers.

Table 4 ThinPAK 5 × 6 matrices and covered area

Via variants	1	2	3	4	5	6	7	8
Via inner	2 × 2	2 × 2	2 × 2	2 × 2	2 × 2	2 × 2	2 × 2	2 × 2
Via pitch inner	1.7 mm	1.7 mm	1.7 mm	1.7 mm	1.7 mm	1.7 mm	1.7 mm	1.7 mm
Via matrix outer	2 × 2	3 × 4	4 × 6	5 × 8	6 × 10	7 × 11	9 × 15	11 × 19
Via pitch outer	1.7 mm	1.7 mm	1.7 mm	1.7 mm	1.7 mm	0.85 mm	0.85 mm	0.85 mm
Covered area (mm^2)	17.2	26	56.9	99.5	153.5	56.9	99.5	153.5
Covered area (percentage)	100	151.2	330.8	578.5	892.4	330.8	578.5	892.4

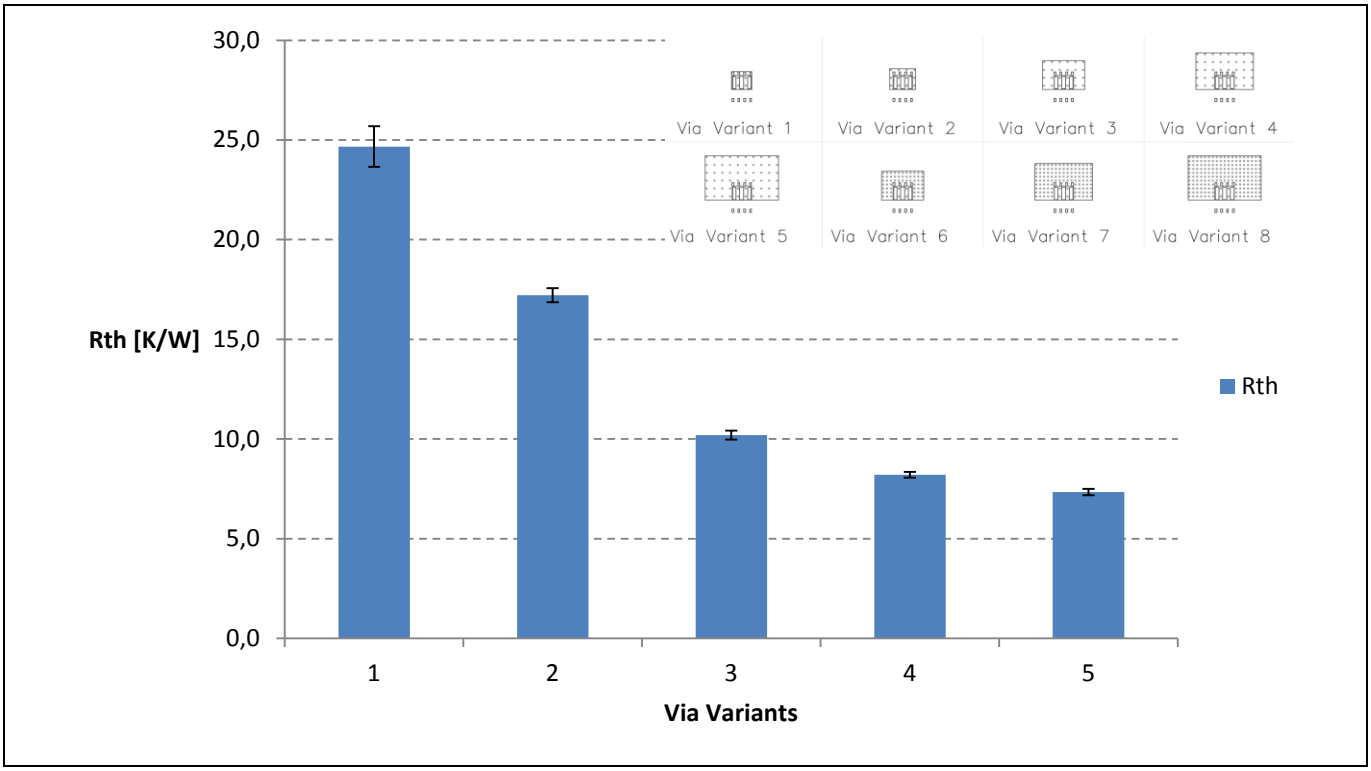


Figure 20 ThinPAK 5x6 V1 to V5 results

The ThinPAK 5x6 shows a similar behavior (shown in Figure 20) as the ThinPAK 8x8, which emphasizes the former results. The measurements show an exponential decrease of the R_{th}. Using Variant 5 instead of Variant 1 decreases the thermal resistance by around 70 percent (24.7 to 7.3 K/W).

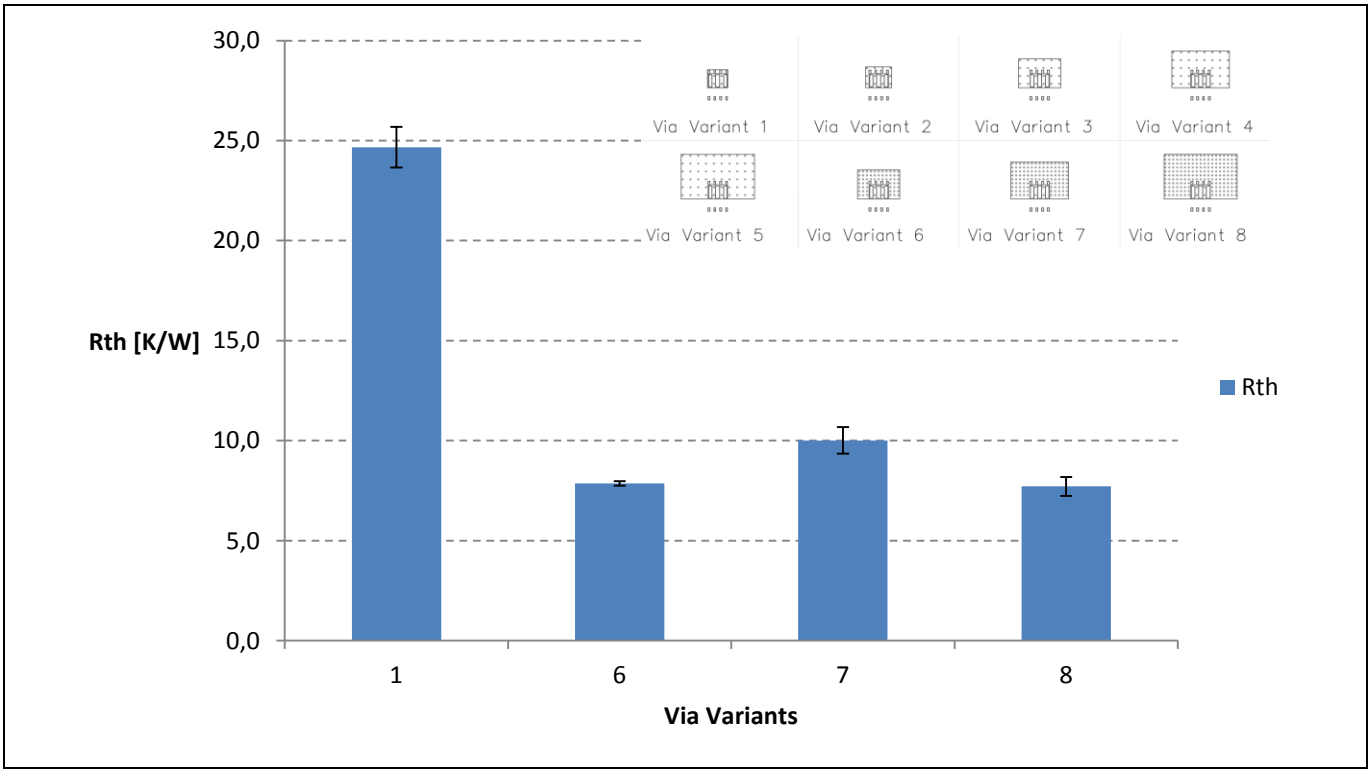


Figure 21 ThinPAK 5x6 V1, V6 to V8 results

Results and interpretation

Using a finer via pitch in Variants 6 to 8 does not lead to a huge gain compared to Variants 1 to 5, as shown in Figure 18. The results for this fine pitch variance are shown in Figure 21. For the ThinPAK 5x6 the same advice can be given as before, for the ThinPAK 8x8 – **use of the less dense via variants leads to a tremendous reduction and is the best choice in terms of cost**.

5.3 DSO

Figure 22 shows the different matrices and the covered areas for Variants 1 to 8.

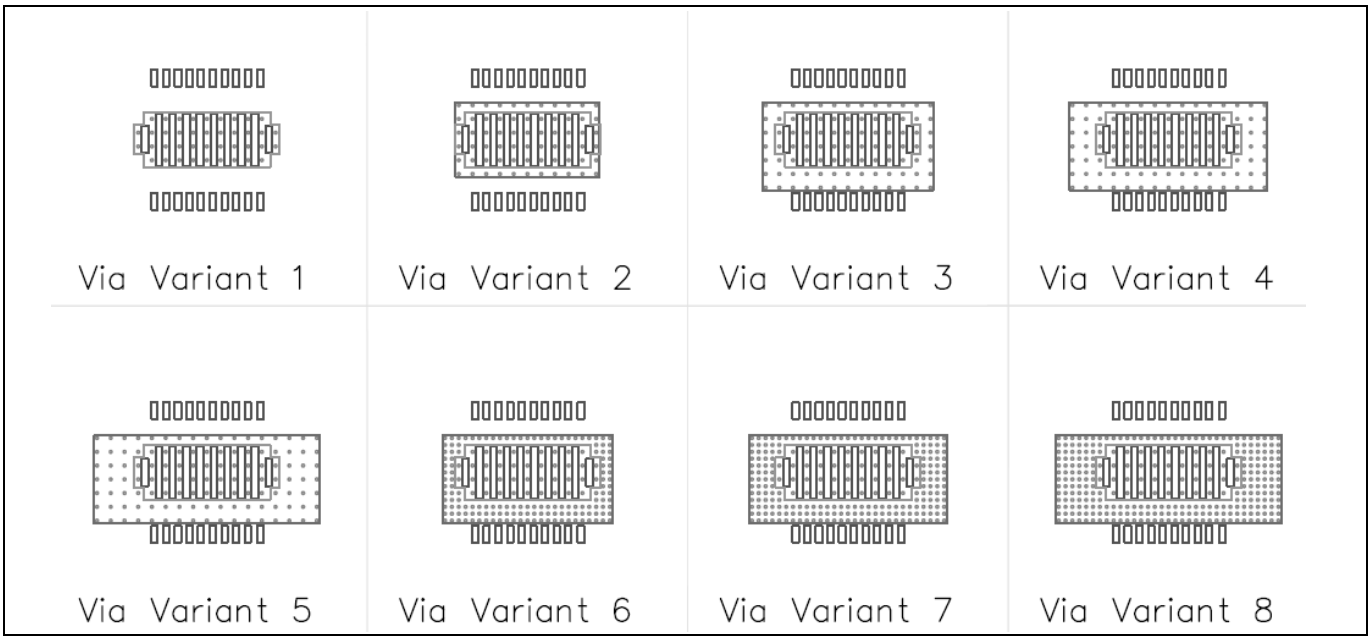


Figure 22 PCB structure DSO-20-85

Table 4 shows the matrices used and the covered areas in absolute and relative numbers.

Table 5 DSO-20-85 matrices and covered area

Via variants	1	2	3	4	5	6	7	8
Via inner	4 × 11	4 × 11	4 × 11	4 × 11	4 × 11	4 × 11	4 × 11	4 × 11
Via pitch inner	1.5 mm	1.5 mm	1.5 mm	1.5 mm	1.5 mm	1.5 mm	1.5 mm	1.5 mm
Via matrix outer	4 × 11	6 × 11	7 × 13	7 × 15	7 × 17	13 × 25	13 × 29	13 × 33
Via pitch outer	1.5 mm	1.5 mm	1.5 mm	1.5 mm	1.5 mm	0.75 mm	0.75 mm	0.75 mm
Covered area (mm^2)	85.1	127.5	178.6	207.4	236.2	178.6	207.4	236.2
Covered area (percentage)	100	149.8	209.9	243.7	277.6	209.9	243.7	277.6

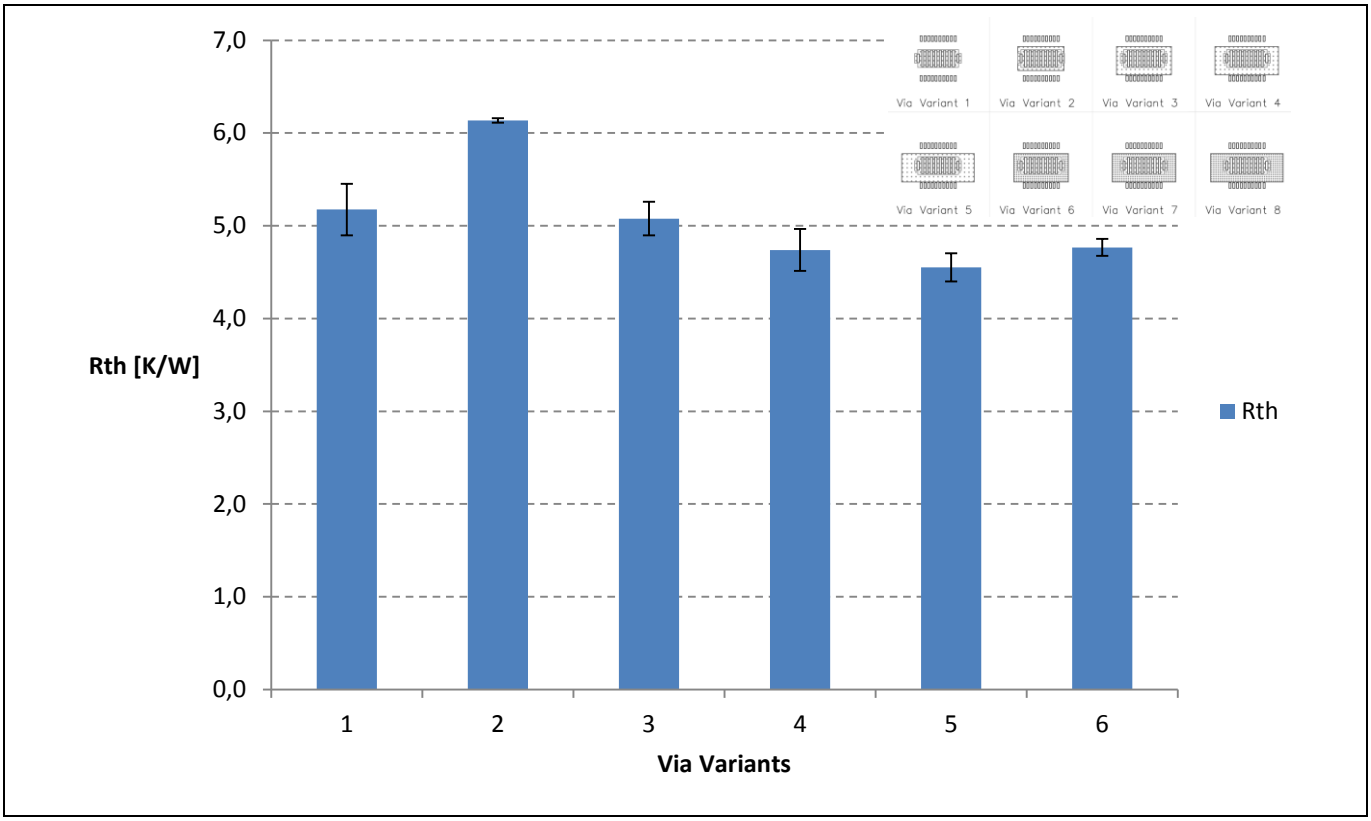


Figure 23 DSO20-85 V1 to V6 results

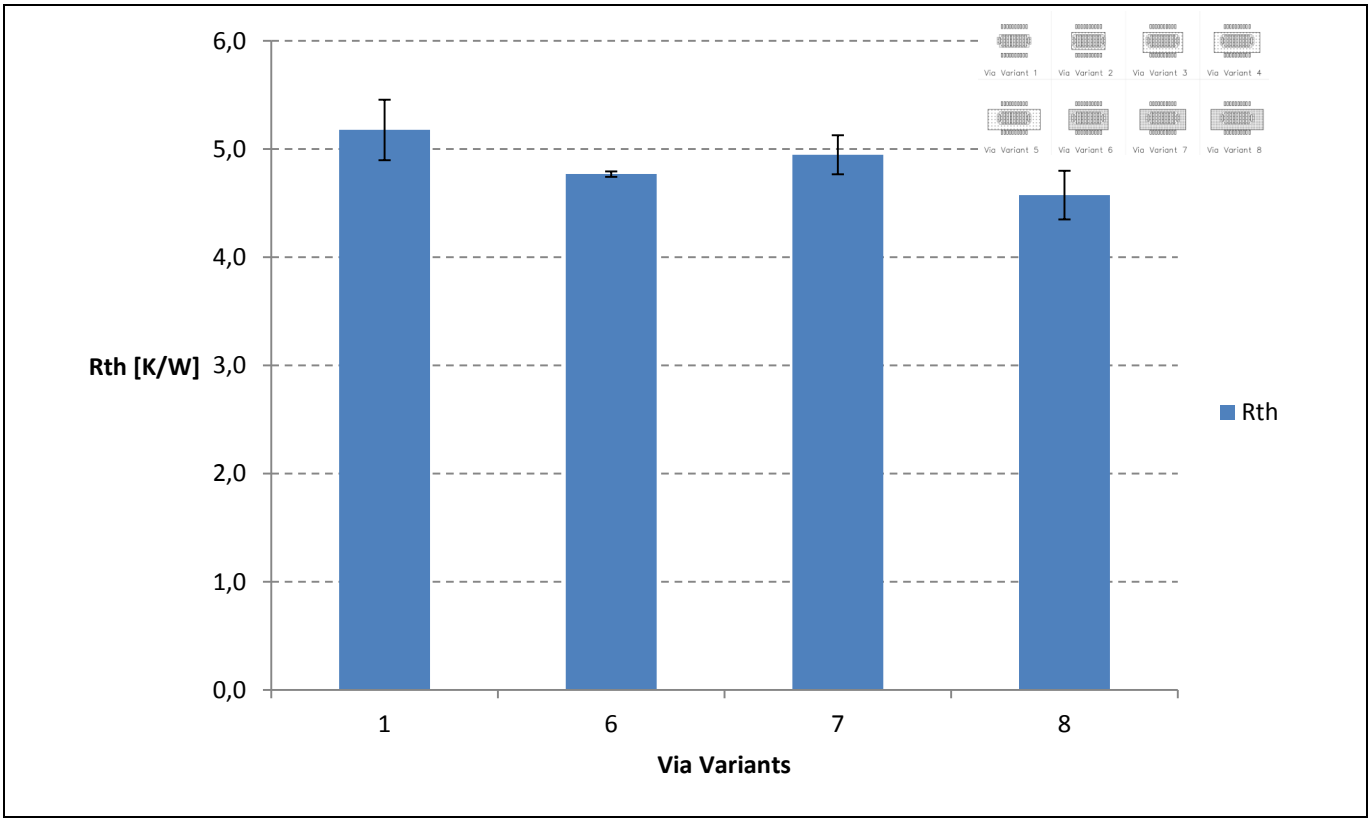


Figure 24 DSO20-85 V1, V6 to V8 results

Results and interpretation

The DSO package may be smaller, depending on the layout represented in Figures 23 and 24.

Our recommendation is to choose the wider via variants, and as the second design parameter consider the available space on the PCB. For designs with space constraints Variant 1 is suitable.

5.4 TOLL G7

Figure 25 presents the via matrices and the covered area for the different variants.

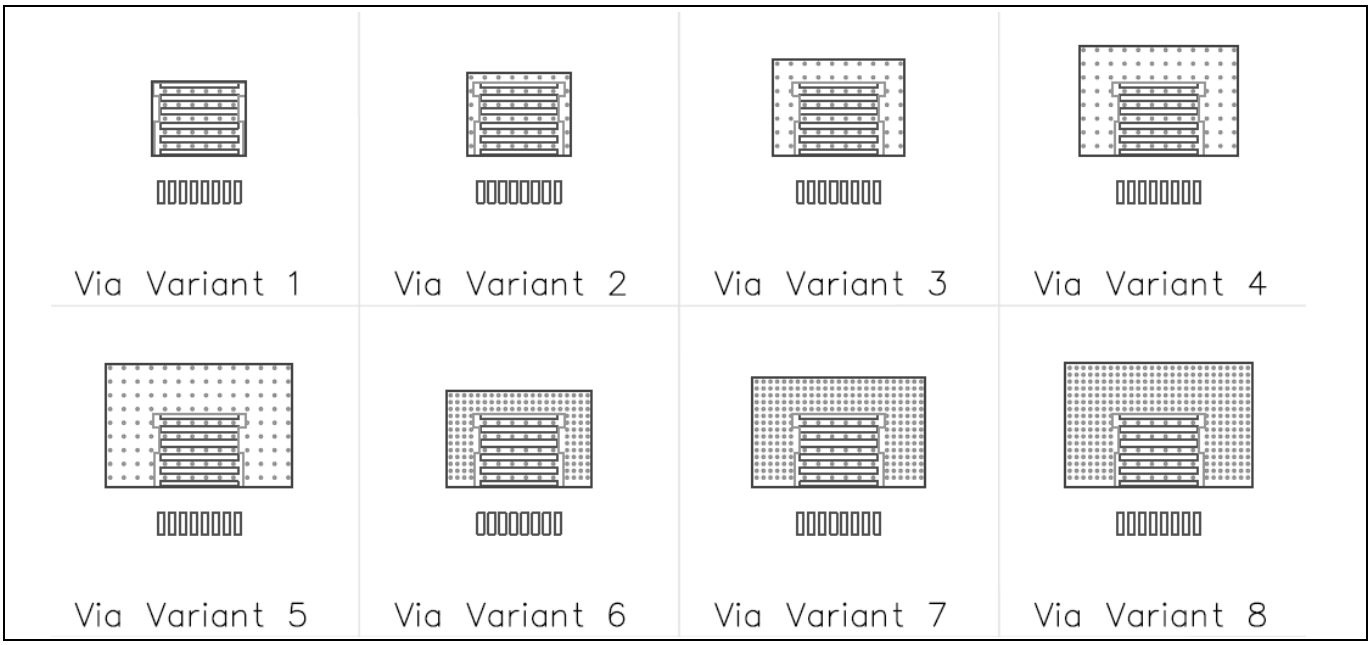


Figure 25 PCB structure TOLL G7

Table 6 shows the matrices used and the covered areas in absolute and relative numbers.

Table 6 TOLL matrices and covered area

Via variants	1	2	3	4	5	6	7	8
Via inner	5 × 6	5 × 6	5 × 6	5 × 6	5 × 6	5 × 6	5 × 6	5 × 6
Via pitch inner	1.5 mm	1.5 mm	1.5 mm	1.5 mm	1.5 mm	1.5 mm	1.5 mm	1.5 mm
Via matrix outer	5 × 6	6 × 8	7 × 10	8 × 12	9 × 14	13 × 21	15 × 25	17 × 27
Via pitch outer	1.5 mm	1.5 mm	1.5 mm	1.5 mm	0.75 mm	0.75 mm	0.75 mm	0.75 mm
Covered area (mm^2)	84.5	103.2	151.9	209.7	276.4	167.7	227.7	278.8
Covered area (percentage)	100	122.1	179.8	248.2	327.1	198.5	269.5	329.9

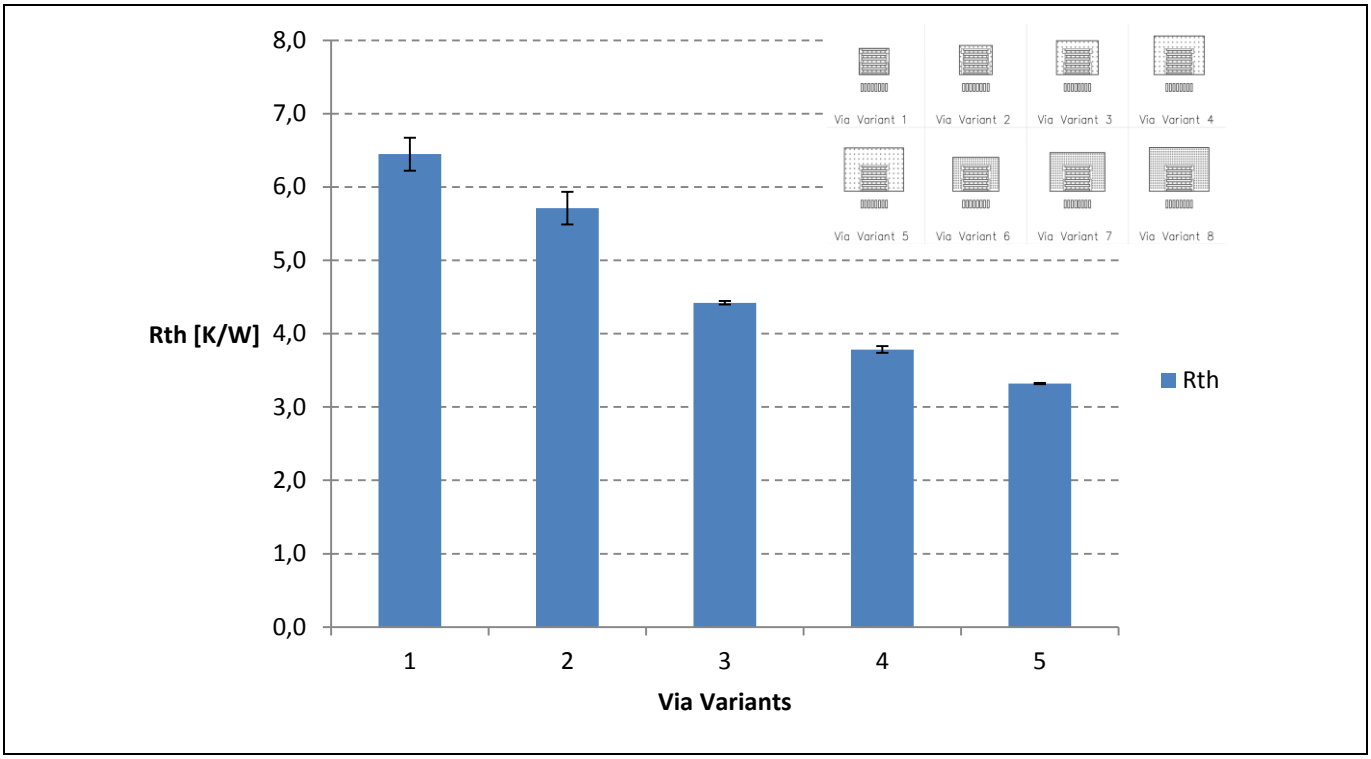


Figure 26 TOLL G7 V1 to V5

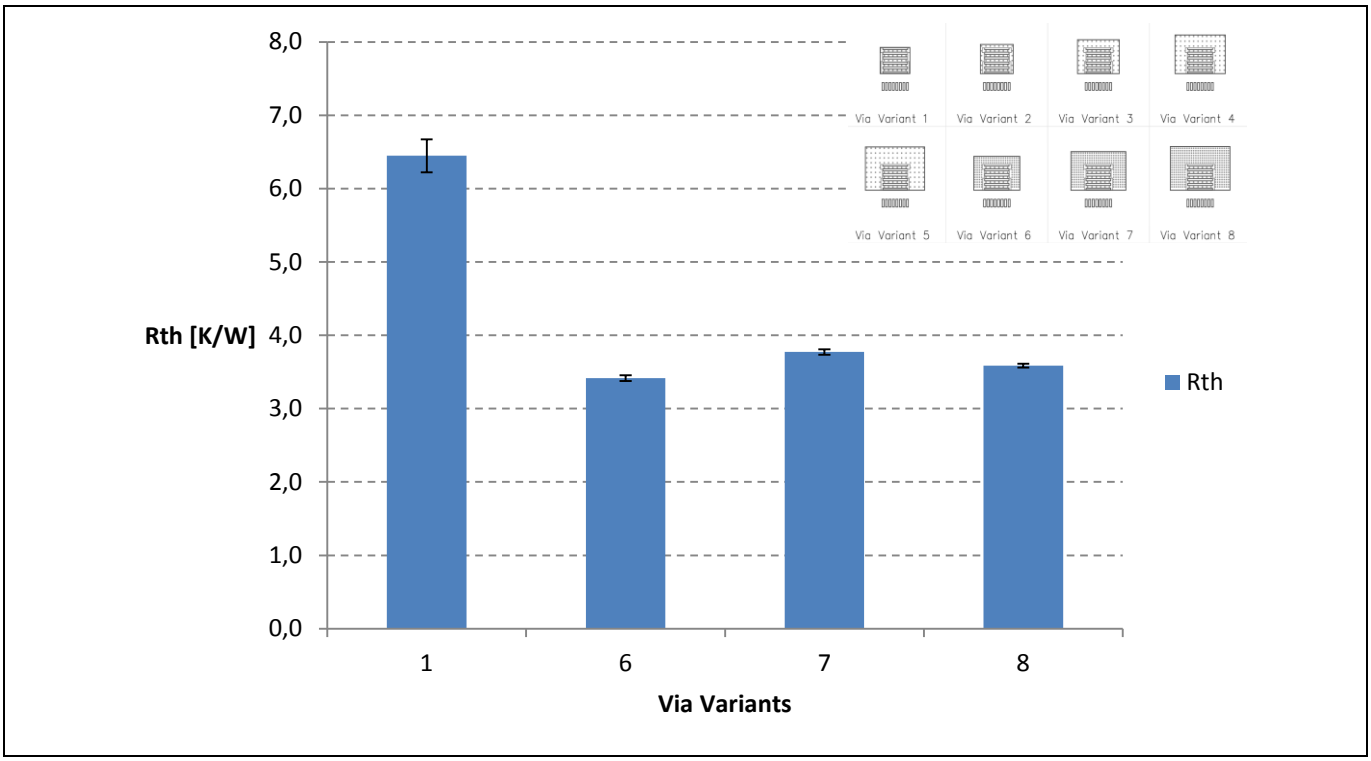


Figure 27 TOLL G7 V1, V6 to V8

TOLL shows a nearly linear behavior in Variants 1 to 5, as shown in Figure 26. A trend toward saturation is not visible. The denser via variants show similar results in Figure 27, leading to the recommendation to **go for the wider via variants shown in Figure 26**.

5.5 TOLL GaN

Figure 28 shows the via matrices and the covered area for the TOLL GaN package.

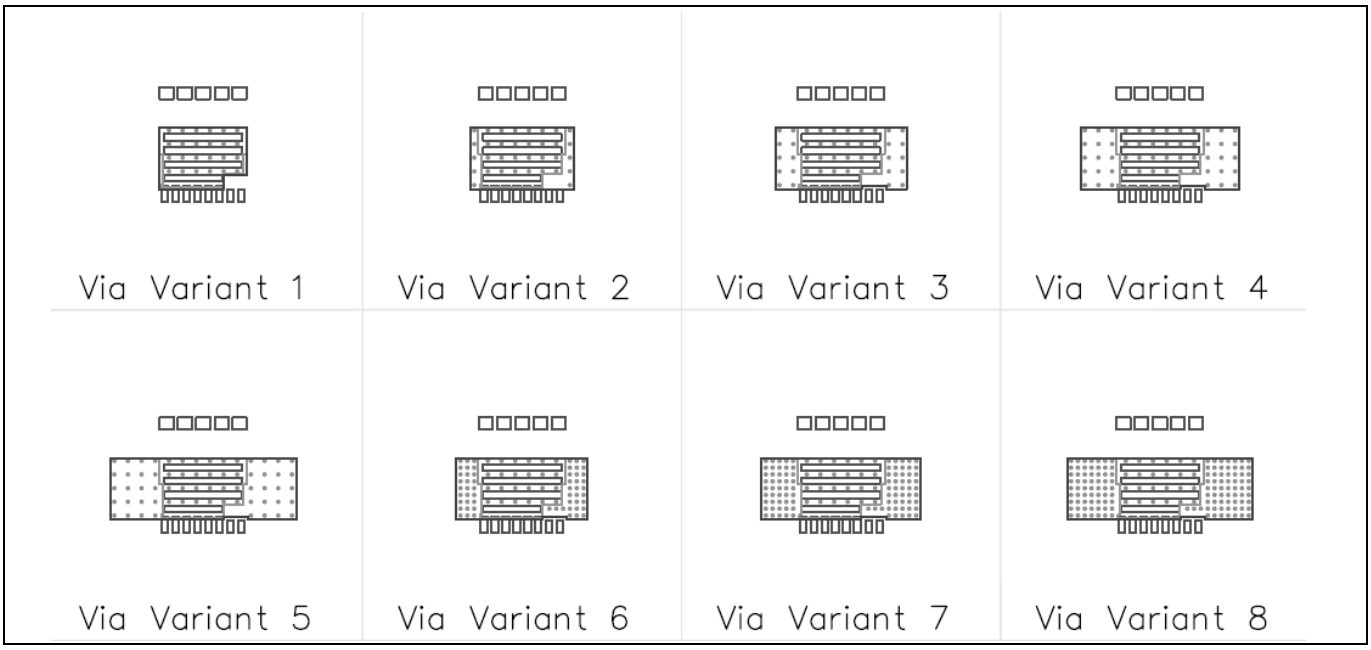


Figure 28 PCB structure TOLL GaN

Table 7 shows the matrices used and the covered areas in absolute and relative numbers.

Table 7 TOLL matrices and covered area

Via variants	1	2	3	4	5	6	7	8
Via inner	4 × 6	4 × 6	4 × 6	4 × 6	4 × 6	4 × 6	4 × 6	4 × 6
Via pitch inner	1.5 mm	1.5 mm	1.5 mm	1.5 mm	1.5 mm	1.5 mm	1.5 mm	1.5 mm
Via matrix outer	4 × 6	5 × 8	5 × 10	5 × 12	5 × 14	4 × 6 + 6 × 9	4 × 6 + 10 × 9	4 × 6 + 14 × 9
Via pitch outer	1.5 mm	1.5 mm	1.5 mm	1.5 mm	1.5 mm	0.75 mm	0.75 mm	0.75 mm
Covered area (mm^2)	65.5	77	97.2	117.5	137.7	97.2	117.5	137.7
Covered area (percentage)	100	117.6	148.4	179.4	210.2	148.4	179.4	210.2

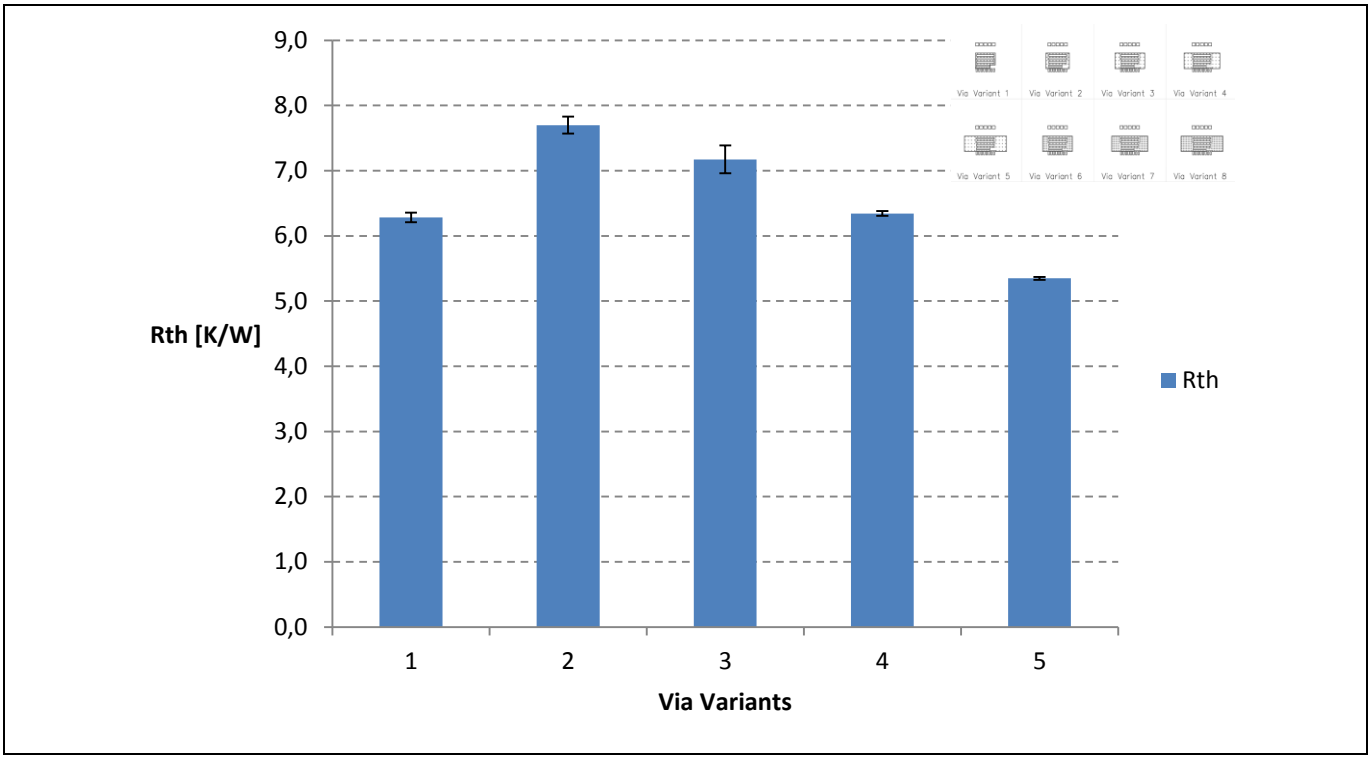


Figure 29 TOLL GaN V1 to V5

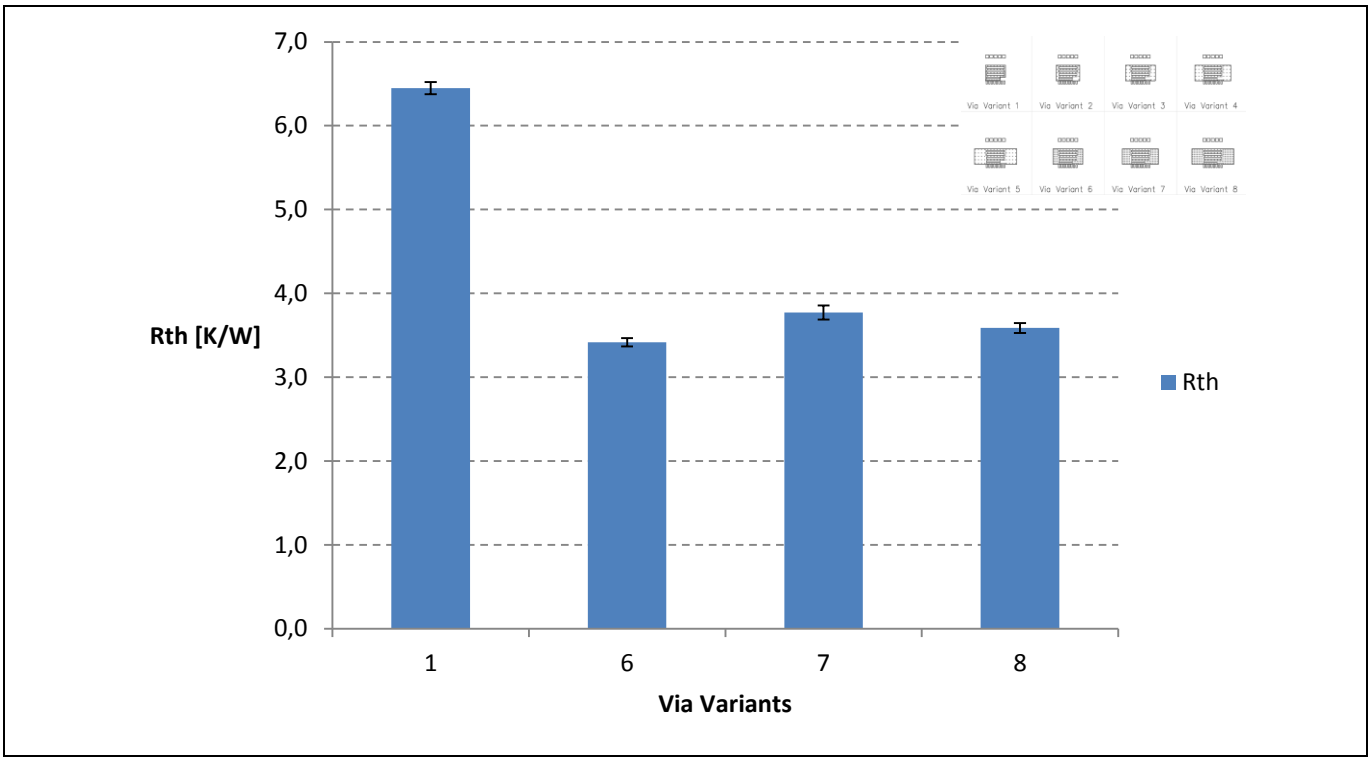


Figure 30 TOLL GaN V1, V6 to V8

Figures 29 and 30 show the results for the GaN TOLL, which is much more dependent on the via variants.

The dense variants 6 to 8 show clear benefits in Figure 30.

6 Conclusion

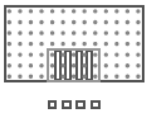
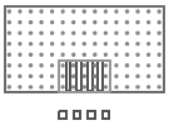
This document worked out the best combinations of package and via matrix on the PCB level to achieve optimal cooling performance. For each package an optimum was found, which is explained in the related paragraphs. Table 8 shows the devices tested and the related packages.

Table 8 Devices tested

Device	Package
IPL65R230C7	PG-VSON-4-1 ThinPAK 8x8
IPL60R360P6S	PG-TSON-8-2 ThinPAK 5x6
IGO60R070D1	PG-DSO-20-85 DSO
IPT65R033G7	PG-HSOF-8-2 TOLL
IGT60R070D1	PG-HSOF-8-2 TOLL

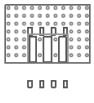
ThinPAK 8x8 showed the best performance with less dense vias, as seen in Variants 5 and 6, shown in Table 9. The difference between these two is marginal. Taking cost into consideration leads to choosing Variant 5, which has fewer vias.

Table 9 ThinPAK 8x8 recommendations

	Variant 5	Variant 6
Via inner	3 × 5	3 × 5
Via pitch inner	1.5 mm	1.5 mm
Via matrix outer	7 × 13	8 × 15
Via pitch outer	1.5 mm	1.5 mm
PCB structure		
Best achievable R_{th}	6 [K/W]	4 [K/W]

ThinPAK 5x6 behaves similarly to the ThinPAK 8x8. The less dense via matrix is preferable, whereby saturation is forseeable. Variant 6 is the best choice in the current setting, as shown in Table 10.

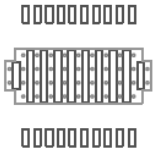
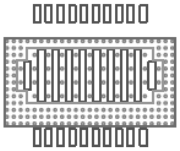
Table 10 ThinPAK 5x6 recommendations

	Variant 6
Via inner	2 × 2
Via pitch inner	1.7 mm
Via matrix outer	7 × 11
Via pitch outer	0.85 mm
PCB structure	
Best achievable R_{th}	7.9 [K/W]

Conclusion

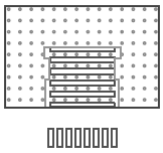
The DSO package performs similarly in the dense via matrices as in the wider ones. Variant 1 for wide variants and Variant 6 for designs with space constraints and optimized thermal resistance are preferable, as shown in Table 11.

Table 11 DSO recommendations

	Variant 1	Variant 6
Via inner	4 × 11	4 × 11
Via pitch inner	1.5 mm	1.5 mm
Via matrix outer	4 × 11	13 × 25
Via pitch outer	1.5 mm	0.75 mm
PCB structure		
Best achievable R_{th}	4.8 [K/W]	4.7 [K/W]

TOLL G7 shows a linear dependency, with the less dense via matrix on the thermal resistance. Variant 5, shown in Table 12, is the best choice in times of performance and cost.

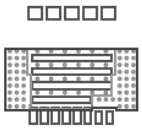
Table 12 TOLL G7 recommendations

	Variant 5
Via inner	5 × 6
Via pitch inner	1.5 mm
Via matrix outer	9 × 14
Via pitch outer	0.75 mm
PCB structure	
Best achievable R_{th}	5.3 [K/W]

TOLL GaN is the only package showing a behavior that makes the dense matrix seen in Variant 6 in Table 13 preferable.

Conclusion

Table 13 TOLL GaN recommendations

	Variant 6
Via inner	4 × 6
Via pitch inner	1.5 mm
Via matrix outer	4 × 6 + 6 × 9
Via pitch outer	0.75 mm
PCB structure	
Best achievable R_{th}	3.3 [K/W]

What can be concluded overall from the results is that each combination of technologies and package must be evaluated separately.

7 References

[1] S. Maniktala: “Switching Power Suppplies A-Z,” Newnes, 2013

[2] General Recommendations for Assembly of Infineon Packages [Online]. Available at: https://www.infineon.com/dgdl/Infineon-General_Recommendations_for_Assembly_of_Infineon_Packages-P-v04_00-EN.pdf?fileId=5546d4625cc9456a015ccaf4a1fe3a32

[3] 500 V–900 V CoolMOS™ N-Channel Power MOSFET homepage: https://www.infineon.com/cms/en/product/power/mosfet/500v-900v-coolmos-n-channel-power-mosfet/

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