18 W adapter power supply for set-top box using ICE5GSAG and IPN70R1K2P7S

REF_5GSAG_18W1

About this document

Scope and purpose

This document is a reference design for an 18 W adapter power supply for a set-top box with the latest fifth-generation Infineon Fixed Frequency (FF) controller (ICE5GSAG) and CoolMOS™ P7 (IPN70R1K2P7S). The power supply is designed with a universal input compatible with most geographic regions, and an isolated output (+12 V/1.5 A) on a single-layer PCB.

Highlights of the adapter for a set-top box are:

- Up to 18 W continuous output power in a universal input voltage range design
- High average efficiency and low standby power to meet the European Union's Code of Conduct (CoC) Version 5 Tier 2 single-voltage external AC-DC power supply basic-voltage requirements
- Comprehensive protection feature controller in DSO-8 package and high ESD ruggedness 700 V CoolMOS™ P7 superjunction MOSFET
- Auto-restart protection scheme to minimize interruption and enhance end-user experience

Intended audience

This document is intended for power supply design engineers who are designing highly efficient power adapters to meet regulatory standards. Do note that the design serves as a means for laboratory evaluation and adaption to other customized design. Thus, no relevant safety and regulatory certification has been submitted and granted for commercial purposes.

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1 System introduction

The standard requirements for external power supply efficiency and standby power set by regulatory bodies are becoming tougher to meet. Some stricter countries implement these standards to be mandatory, while elsewhere they are voluntary. Therefore, power supply designers needs to quickly adapt to ensure that their designs are in compliance with these standards. To support this trend, Infineon has introduced the fifth-generation FF controller to address the need for highly efficient and low standby power adapter power supplies in a cost-effective manner.

The adapter power supply is needed to power various modules and processors, which typically operate from a stable DC voltage source. The Infineon FF controller (ICE5GSAG) with the CoolMOS™ P7 (IPN70R1K2P7S) forms the heart of the power supply system, providing necessary protection and AC-DC conversion from the mains to single regulated DC voltage to power various blocks.

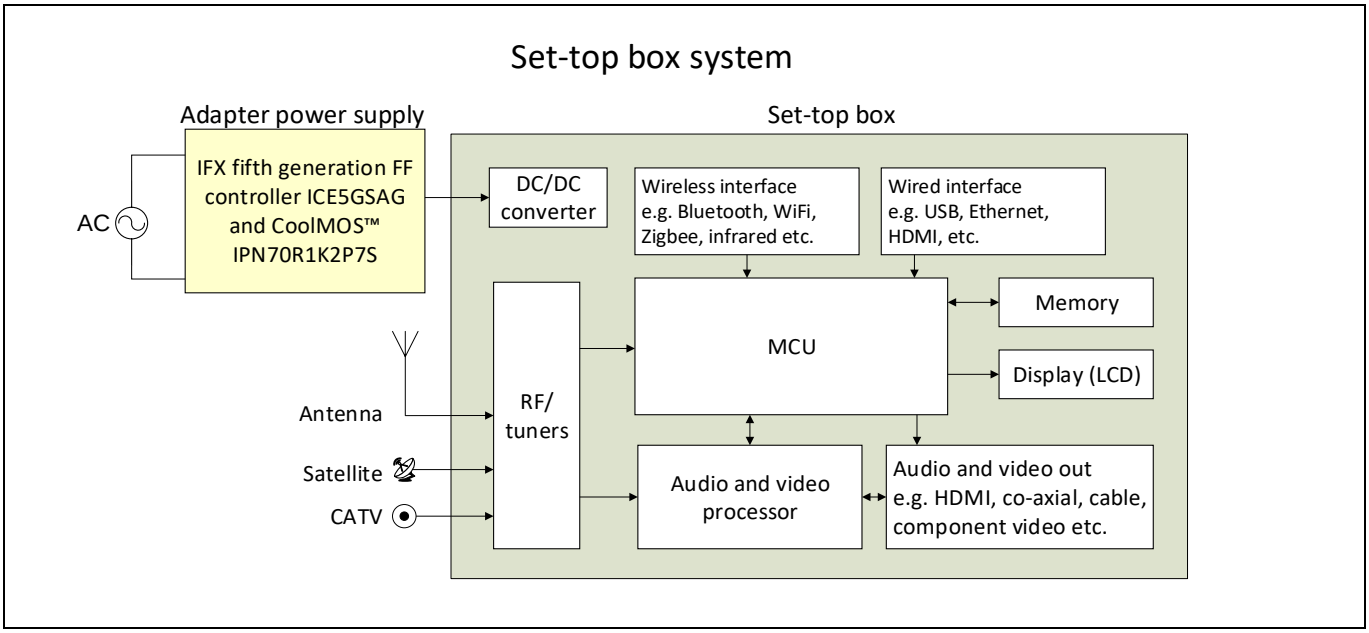


Figure 1 Simplified set-top box system block diagram example

Table 1 lists the system requirements for an adapter power supply for a set-top box, and the corresponding Infineon solution is shown in the right-hand column.

Table 1 System requirements and Infineon solutions

	System requirement for adapter power supply	Infineon solution – ICE5GSAG and IPN70R1K2P7S
1	High average efficiency and low standby power to meet CoC Tier 2 requirements	New FF control and Active Burst Mode (ABM) with extremely low-loss CoolMOS™
2	Robust system and protection features	Comprehensive protection feature controller in DSO-8 package and high ESD ruggedness 700 V CoolMOS™ P7
3	Auto-restart protection scheme to minimize interruption and enhance end-user experience	All protections are in auto-restart

1.1 High average efficiency and low standby power to meet CoC Tier 2 requirement

There are currently two common standards regulating the efficiency of External Power Supplies (EPS), namely United States Department of Energy (DoE) Level VI and EU European Code of Conduct (CoC) Version 5 Tier 2. They are largely similar in terms of regulating efficiency at various load conditions as well as no-load standby power. However, EU CoC Tier 2 has a more stringent specification as well as an additional loading condition to be considered. At the point of writing, only DoE Level VI has been made mandatory for all EPS imported into the United States since February 2016.

In this 18 W reference design with an output of 12 V and 1.5 A, using the efficiency formula outlined in the EU CoC Tier 2 specification, the EPS need to achieve an average efficiency of 85.45 percent and an efficiency of 75.46 percent at 10 percent load condition measured at rated voltage. In addition, a no-load power draw of not more than 75 mW is required.

In comparison with DoE Level VI, the EPS need to achieve an average efficiency of 85 percent and a no-load power draw of not more than 100 mW. As such, the content of the following document will simply focus on stringent standards relating to the above two cases.

During typical set-top box operation, the power requirement fluctuates according to various use cases. Therefore, the efficiency should be optimized throughout the load range. To achieve the average efficiency requirement, the controller should be able to adapt and adjust its switching operation according to the output load. During standby state, the set-top box only consumes very minimal power. It is crucial that the adapter power supply operates as efficiently as possible, because it will be in this particular state for most of the day.

In this reference design, ICE5GSAG was primarily chosen due to its frequency-reduction switching scheme and ABM. Compared with a traditional FF flyback, the controller reduces its switching frequency from medium to light load, thereby minimizing switching losses. Further reduction in load will trigger the controller to operate in ABM for a more efficient operation. Therefore, an average efficiency of more than 86 percent is achievable under nominal line input conditions.

ICE5GSAG supports CCM operation enhanced with slope compensation for stable operation. The system is designed to operate at CCM during heavy load and low input voltage to improve efficiency by reducing the conduction losses through reduction of RMS currents.

In addition to the frequency-reduction scheme, ABM and CCM operation, the low switching losses introduced by the latest 700 V CoolMOS™ P7 (IPN70R1K2P7S) and its small-package SOT-223 enables the adapter power supply to meet the highest efficiency standards and support the high power density.

1.2 Robust system and protection features

Comprehensive protection features are integrated into the FF controller ICE5GSAG such as input Line Over Voltage Protection (LOVP), V_{CC} Over Voltage (OV), V_{CC} Under Voltage (UV), over-load/open-loop, over-temperature and Current Sense (CS) short-to-GND. It also has limited charging current for V_{CC} short-to-GND.

The 700 V CoolMOS™ P7 (IPN70R1K2P7S) has an integrated ESD protection diode for high ESD ruggedness and robust system requirements.

1.3 Auto-restart protection scheme to minimize interruption and enhance end-user experience

For an adapter power supply, it would be annoying to both the end user and the manufacturer if the system were to halt and latch after protection. To minimize interruption, the controller implements auto-restart mode for all protections.

2 Reference design board

This document provides complete design details including specifications, schematics, Bill of Materials (BOM), PCB layout, and transformer design and construction information. Performance results pertaining to line/load regulation, efficiency, transient load, thermal conditions, conducted EMI scans and so on are also included.

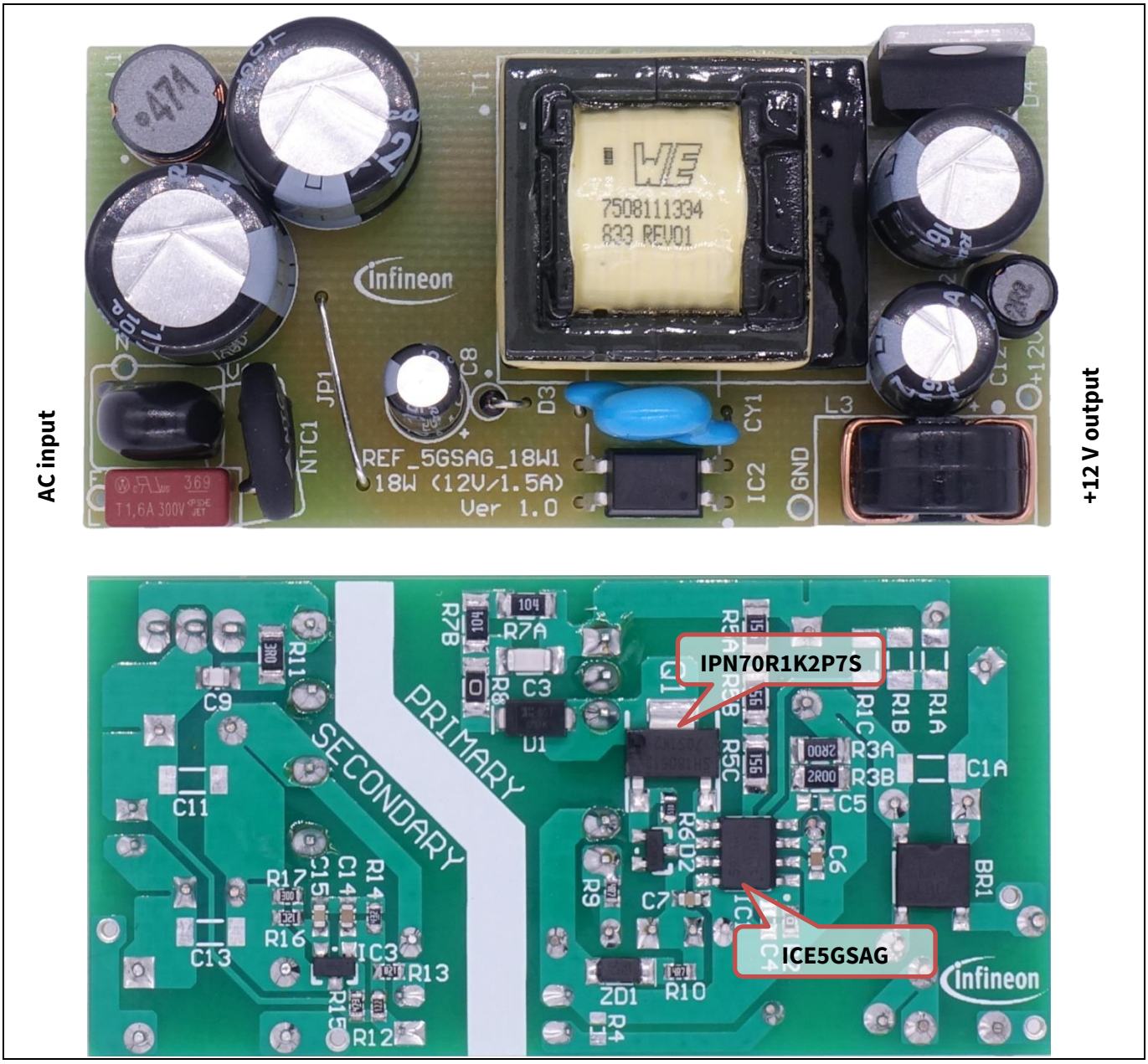


Figure 2 REF_5GSAG_18W1

3 Power supply specifications

The table below represents the minimum acceptance performance of the design at 25°C ambient temperature. Actual performance is listed in the measurements section.

Table 2 Specifications of REF_5GSAG_18W1

Description	Symbol	Min.	Type	Max.	Units	Comments
Input						
Voltage	V_{IN}	90	–	265	V AC	2 wires (no P.E.)
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load input power	P_{stby_NL}	–	–	40	mW	230 V AC
In-rush current	I_{Inrush}	–	–	60	A	230 V AC
Leakage current	I_{leak}	–	–	0.25	mA	
Output						
Output voltage	V_{OUT}	–	12	–	V	± 2 percent (PCB end)
Output current	I_{OUT}	–	–	1.5	A	
Output power	P_{OUT_Nom}	–	–	18	W	
Output voltage ripple	V_{RIPPLE}	–	–	100	mV	20 MHz bandwidth
Output over-current protection	I_{OCP}	1.8	–	2.7	A	
Start-up time	t_{start_up}	–	–	250	ms	
Hold-up time	t_{hold_up}	15	–	–	ms	115 V AC/230 V AC
Efficiency (cable end)						
Maximum load	η	86	–	–	%	115 V AC/230 V AC
Average efficiency (25 percent, 50 percent, 75 percent, 100 percent)	η_{avg}	86	–	–	%	115 V AC/230 V AC
10 percent load efficiency	$\eta_{10\%}$	80	–	–	%	115 V AC/230 V AC
Environmental						
Conducted EMI			10		dB	Margin, CISPR 22 class B
ESD						EN 61000-4-2
Contact discharge			±8		kV	
Air discharge			±15		kV	
Surge immunity						EN 61000-4-5
Differential Mode (DM)			±1		kV	
Common Mode (CM)			±4		kV	
Form factor (PCB assembly)			66 x 33 x 21		mm^3	L x W x H (single-layer PCB)

Note: 1.5 m long 0.5 mm^2 x 2C wire adapter cable is used.

4 Circuit diagram

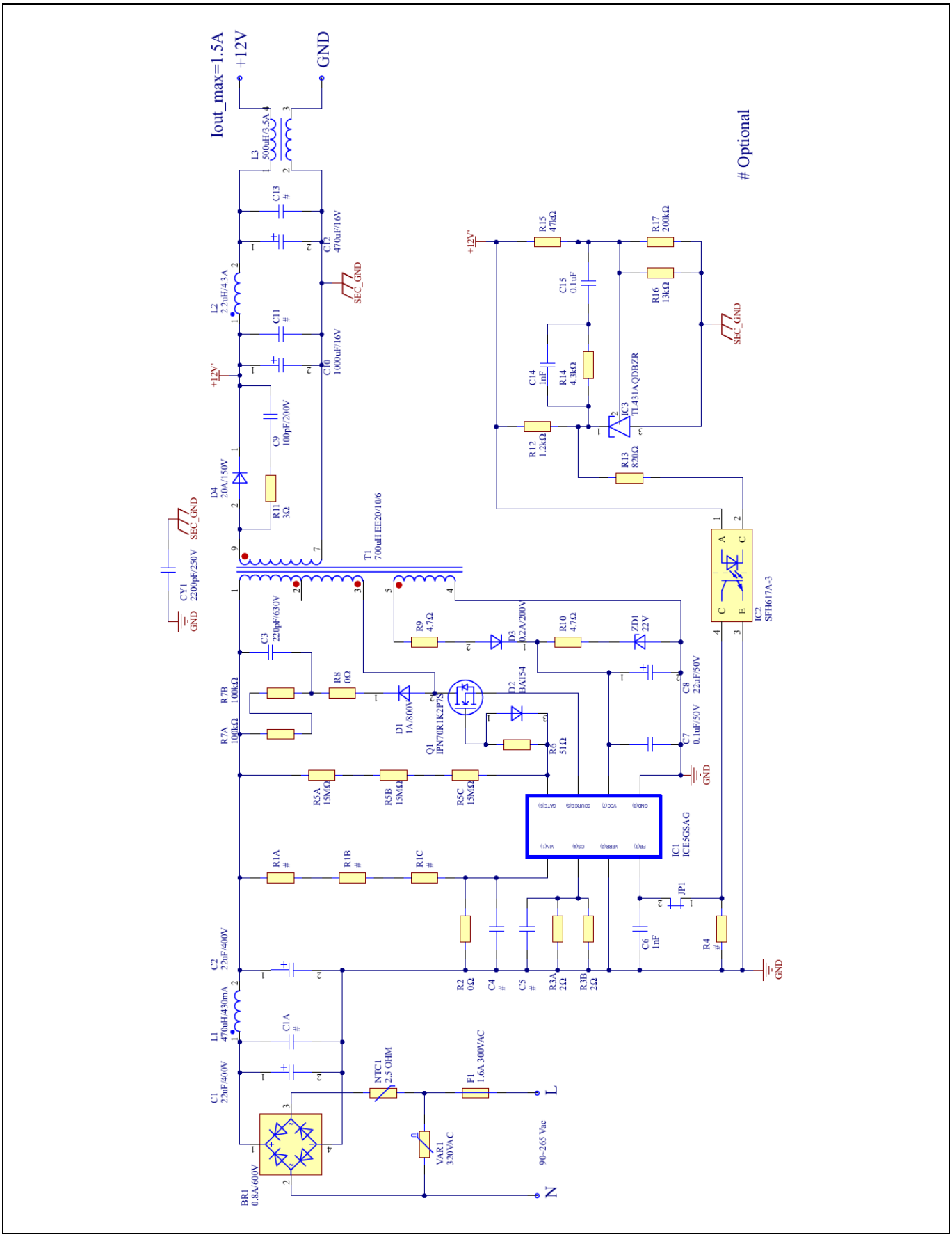


Figure 3 Schematic of REF_5GSAG_18W1

5 Circuit description

In this section, the design circuit for the SMPS unit will be briefly described by the different functional blocks. For details of the design procedure and component selection for the flyback circuitry please refer to the IC design guide [3] and calculation tool [4].

5.1 EMI filtering and line rectification

The input of the power supply unit is taken from the AC power grid, which is in the range of 90 V AC ~ 265 V AC. The fuse F1 is directly connected to the input line to protect the system in case of excess current entering the system circuit due to any fault. Following is the varistor VAR1, which is connected across the input to absorb excessive energy during line surge transient. Resistor NTC1 not only reduces the in-rush current during start-up, but it also helps reduce the voltage increase on the bulk capacitors C1 and C2 during line surge transients. The bridge rectifier BR1 rectifies the AC input into DC voltage, filtered by the bulk capacitors C1 and C2. Inductor L1 and capacitors C1 and C2 form a π filter to attenuate EMI noise.

5.2 Flyback converter power stage

The flyback converter power stage consists of transformer T1, a primary HV MOSFET Q1, secondary rectification diode D4, secondary output capacitors C10 and C12, and output filter inductor L2.

When the primary HV MOSFET turns on, energy is stored in the transformer. When it turns off, the stored energy is discharged to the output capacitors and into the output load.

Secondary winding is sandwiched between two layers of primary winding to reduce leakage inductance. This improves efficiency and reduces voltage spikes. An addition of shield winding between the first layer of primary winding and secondary winding helps reduce EMI noise.

For the output rectification, lower forward voltage and ultra-fast recovery diodes can improve efficiency. Capacitor C10 stores the energy needed during output load jumps. LC filter L2/C12 and output CMC L3 reduce the HF ripple voltage.

5.3 Control of flyback converter through fifth-generation FF controller ICE5GSAG

5.3.1 Current Sensing (CS)

The ICE5GSAG is a CM controller. The primary peak current is controlled cycle-by-cycle through the CS resistors R3A and R3B in the CS pin (pin 4). Transformer saturation can be avoided through Peak Current Limitation (PCL), meaning the system is more protected and reliable.

5.3.2 Feedback (FB) and compensation network

V_{OUT} is sensed by resistor dividers R15, R16 and R17, connected to the input of error amplifier TL431 (IC3). A type 2 compensation network (C14, C15 and R14) is connected to the input and output of IC3. The output of IC3 is coupled to the FB pin via optocoupler IC2.

The FB pin of ICE5GSAG is a multi-function pin which is used to select the entry/exit burst power level through a resistor at the FB pin (R4) and also the burst-on/burst-off sense input during ABM.

5.4 Unique features of the fifth-generation FF controller ICE5GSAG

5.4.1 Fast self-start-up and sustaining of V_{CC}

The IC uses a cascode structure to fast-charge the V_{CC} capacitor. Pull-up resistors R5A, R5B and R5C connected to the gate pin (pin 6) are used to initiate the start-up phase. At first, 0.2 mA is used to charge the V_{CC} capacitor from 0 V to 1.1 V. This is a protection which reduces the power dissipation of the power MOSFET during V_{CC} short-to-GND condition. Thereafter, a much higher charging current of 3.2 mA will charge the V_{CC} capacitor until the V_{CC_ON} is reached. Start-up time of less than 250 ms is achievable with a V_{CC} capacitor of 22 µF.

After start-up, the IC V_{CC} supply is sustained by the auxiliary winding of transformer TR1, which needs to support the V_{CC} to be above Under Voltage Lockout (UVLO) voltage (10 V typ.) through the rectifier circuit R9, D3 and C8.

5.4.2 CCM, DCM operation with frequency reduction

ICE5GSAG can be operated in either Discontinuous Conduction Mode (DCM) or Continuous Conduction Mode (CCM) with frequency-reduction features. This reference board is designed to operate in CCM at low input voltage. When the system is operating at high output load, the controller will switch at 125 kHz fixed frequency. In order to achieve a better efficiency between light load and medium load, frequency reduction is implemented as a function of V_{FB}, as shown in Figure 4. Switching frequency will not reduce further once the minimum switching frequency of 53 kHz is reached.

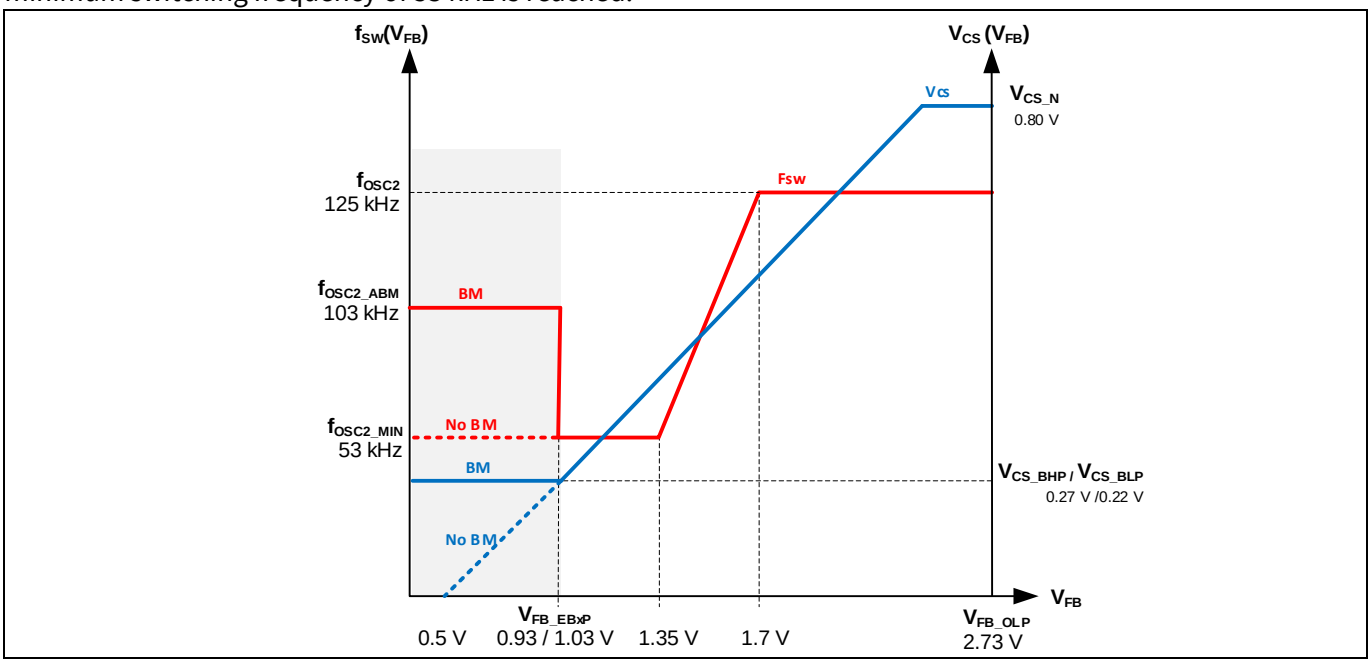


Figure 4 Frequency-reduction curve

5.4.3 Frequency jittering with modulated gate drive

The ICE5GSAG has a frequency jittering feature with modulated gate drive to reduce the EMI noise. The jitter frequency is internally set at 125 kHz (±5 kHz), and the jitter period is 4 ms.

5.4.4 System robustness and reliability through protection features

Protection is one of the major factors in determining whether the system is safe and robust – therefore sufficient protection is necessary. ICE5GSAG provides comprehensive protection to ensure the system is operating safely. This includes V_{IN} LOVP, V_{CC} OV and UV, over-load, over-temperature, CS short-to-GND and V_{CC} short-to-GND. When those faults are found, the system will enter protection mode. Once the fault is removed,

the system resumes normal operation. A list of protections and the failure conditions is shown in the table below.

Table 3 Protection functions of ICE5GSAG

Protection function	Failure condition	Protection mode
V_{CC} OV	V_{VCC} greater than 25.5 V	Odd-skip auto-restart
V_{CC} UV	V_{VCC} less than 10 V	Auto-restart
V_{IN} LOVP	V_{VIN} greater than 2.85 V	Non-switch auto-restart
Over-load	V_{FB} greater than 2.75 V and lasts for 54 ms	Odd-skip auto-restart
Over-temperature	T_J greater than 140°C	Non-switch auto-restart
CS short-to-GND	V_{CS} less than 0.1 V, lasts for 0.4 µs and three consecutive pulses	Odd-skip auto-restart
V_{CC} short-to-GND (V_{VCC} = 0 V, start-up = 50 MΩ and V_{DRAIN} = 90 V)	V_{VCC} less than 1.1 V, $I_{VCC\_Charge1}$ ≈ -0.2 mA	Cannot start up

5.5 Clamper circuit

A clamper network consisting of D1, C3, R7A, R7B and R8 is used to reduce the switching voltage spikes across the MOSFET Q1, which are generated by the leakage inductance of the transformer T1. This is a dissipative circuit; therefore, R7A, R7B and C3 need to be fine-tuned depending on the voltage derating factor and efficiency requirement.

5.6 PCB design tips

For a good PCB design layout, there are several points to note.

- The switching power loop needs to be as small as possible (see Figure 5). There are two power loops in the reference design; one on the primary side and one on the secondary side. The primary-side loop starts from the bulk capacitor (C2) positive terminal, and goes to the primary transformer winding (pin 1 and pin 3 of T1), MOSFET, controller, CS resistors and back to the C2 negative terminal. The secondary-side loop starts at the secondary transformer winding (pin 14 of T1), and goes to output diode D4, output capacitor C10 and back to pin 10 of T1.

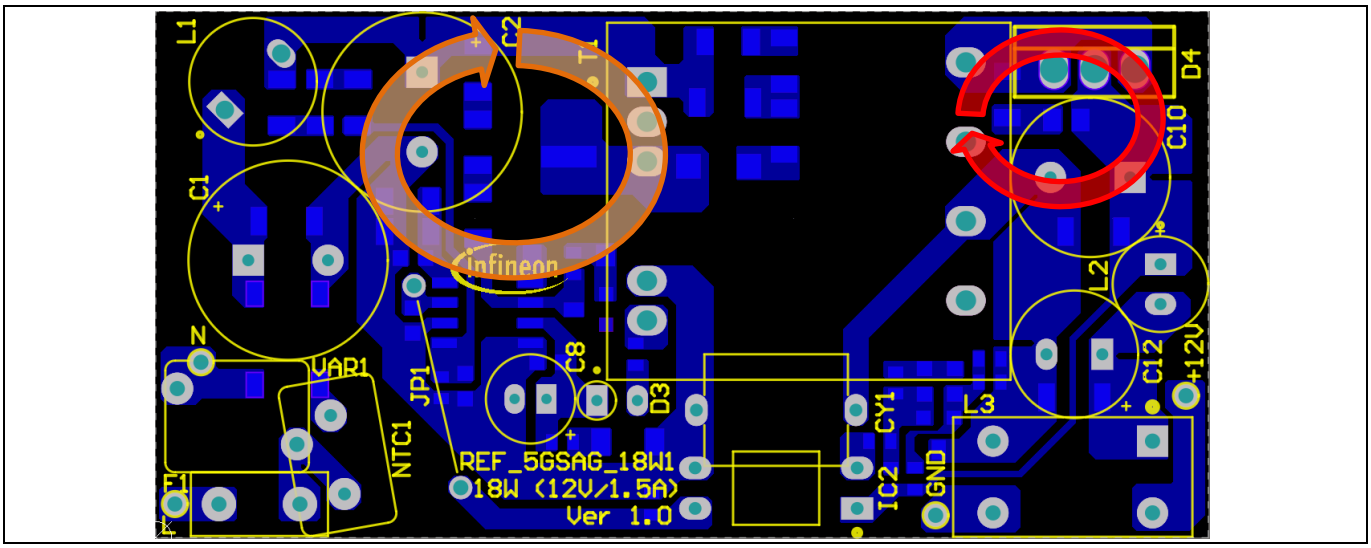


Figure 5 PCB layout tips

- Star-ground connection should be used to reduce HF noise coupling that can affect the functional operation. The ground of the small-signal components, e.g. R2, R4, C4, C5, C6 and C7, and the emitter of the optocoupler (pin 3 of IC2) should connect directly to the IC ground (pin 8 of IC1).
- Separating the HV components and LV components, e.g. clamper circuit (D1, C3, R7A, R7B and R8) at the top part of the PCB, and the other LV components at the lower part of the PCB, can reduce the spark-over chance of the high energy surge during ESD or a lightning surge test.
- Pour the PCB copper over the drain pin of the MOSFET across as wide an area as possible to act as a heatsink.

5.7 EMI reduction tips

EMI compliance is always a challenge for the power supply designer. There are several critical points to consider in order to achieve a satisfactory EMI performance.

- A proper transformer design can significantly reduce EMI. Low leakage inductance can incur a low switching spike and HF noise. Interlaced winding technique is the most common practice to reduce leakage inductance. Winding shield, core shield and whole transformer shield are also some of the techniques used to reduce EMI.
- An input CMC and X-capacitor greatly reduces EMI but it is costly and impractical, especially for low-power applications. There is no input CMC and X-capacitor used in this reference design; therefore, standby power is improved by eliminating the use of an X-capacitor discharge resistor.
- A short-switching power-loop design in the PCB (as described in section 5.6) can reduce radiated EMI due to the antenna effect.
- The Y-capacitor CY1 dampens the HF noise generated between the primary and secondary, reducing the EMI noise.
- The secondary diode snubber circuit (R11 and C9) can reduce HF noise.
- Ferrite beads can reduce HF noise especially at critical nodes such as the drain pin, clamper diode and secondary diode terminals. There is no ferrite bead used in this design, as this can reduce the efficiency due to additional losses especially on the MOSFET and the secondary diode.
- The addition of output CMC (L3) is also effective where long cable wires are used to connect the output of the power supply to the load.

6 PCB layout

6.1 Top side

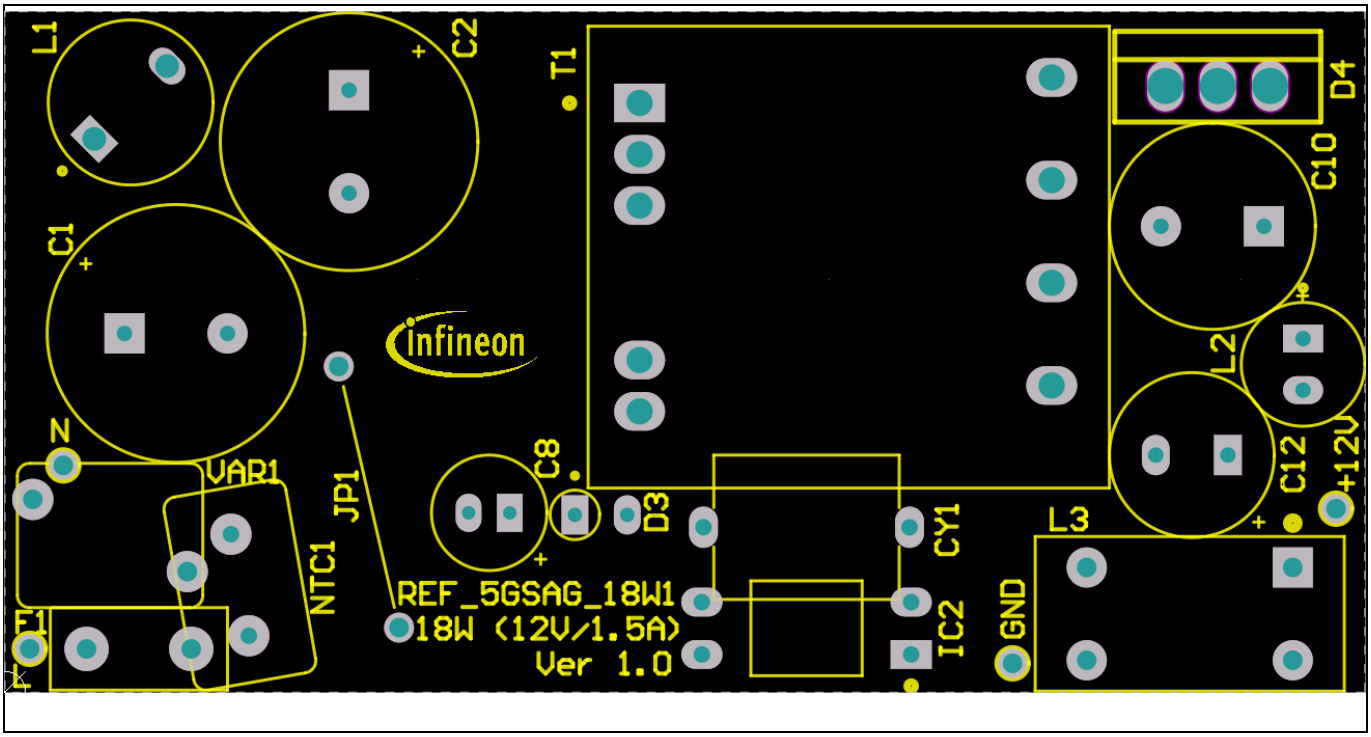


Figure 6 Top-side component legend

6.2 Bottom side

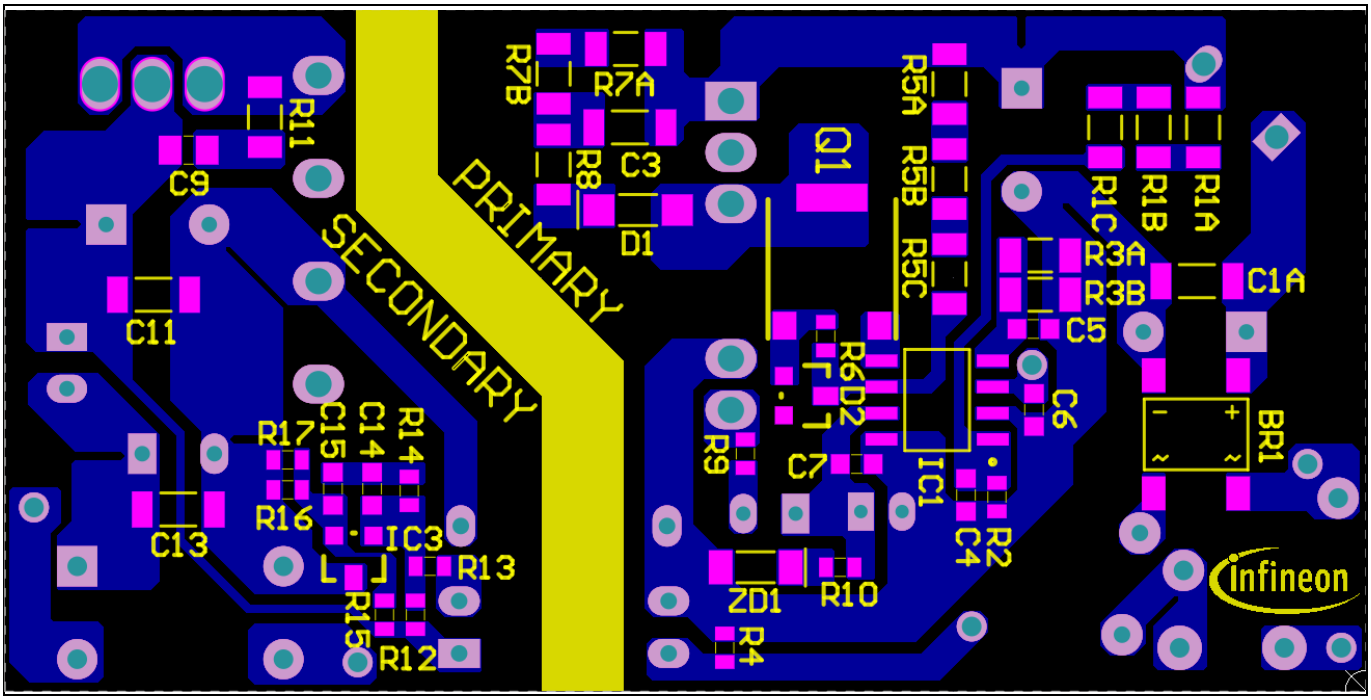


Figure 7 Bottom-side copper and component legend

7 BOM

Table 4 BOM

No.	Designator	Description	Part number	Manufacturer	Quantity
1	BR1	600 V/0.8 A	LMB6S-TP		1
2	C1, C2	22 µF/400 V	400AX22MEFC12.5X16	Rubycon	2
3	C3	220 pF/630 V/1206			1
4	C1A, C4, C5, C11, C13	Not mounted			
5	C6, C14	1 nF/50 V/0603			2
6	C7, C15	100 nF/50 V/0603			1
7	C8	22 µF/50 V	50PX22MEFC5X11	Rubycon	1
8	C9	100 pF/200 V/0805			1
9	C10	1000 µF/16 V	16ZLH1000MEFC10X16	Rubycon	1
10	C12	470 µF/16 V	16ZLH470MEFC8X11.5	Rubycon	1
11	CY1	2200 pF/250 V/X1/Y1	DE1E3KX222MA4BN01F	Murata	1
12	D1	1 A/800 V	US1K-13-F		1
13	D2	200 mA/30 V	BAT54		1
14	D3	0.2 A/200 V	1N485B		1
15	D4	20 A/150 V	MBR20H150CTG	Onsemi	1
16	F1	1.6 A/300 V	36911600000	Littlefuse	1
17	IC1	FF flyback controller	ICE5GSAG	Infineon	1
18	IC2	Optocoupler	SFH617A-3		1
19	IC3	2.5 V_{ref}	TL431AQDBZR		1
20	JP1	13 mm	Jumper		1
21	L1	470 µH/430 mA	744772471	Wurth Electronics	1
22	L2	2.2 µH/4.3 A	7447462022	Wurth Electronics	1
23	L3	400 µH/4.5 A	7448014501	Wurth Electronics	1
24	NTC1	Thermistor, ICL NTC, 2.5 Ω	B57236S0259M000	Epcos	1
25	Q1	1.2 Ω/700 V	IPN70R1K2P7S	Infineon	1
26	R1A, R1B, R1C, R4	Not mounted			
27	R2	0 Ω/0603			1
28	R3A, R3B	2 Ω/0.25 W/1 percent/1206			2
29	R5A, R5B, R5C	15 MΩ/0.25 W/5 percent/1206	RC1206JR-0715ML	Yageo	3
30	R6	51 Ω/0.1 W/5 percent/0603			1
31	R7A, R7B	100 kΩ/0.25 W/5 percent/1206			2
32	R8	0 Ω/1206			1
33	R9, R10	4.7 Ω/0.1 W/5 percent/0603			2
34	R11	3 Ω/0.25 W/5 percent/1206			1
35	R12	1.2 kΩ/0.1 W/5 percent/0603			1
36	R13	820 Ω/0.1 W/5 percent/0603			1
37	R14	4.3 kΩ/0.1 W/5 percent/0603			1
38	R15	47 kΩ/0.1 W/1 percent/0603			1
39	R16	13 kΩ/0.1 W/1 percent/0603			1
40	R17	200 kΩ/0.1 W/1 percent/0603			1
41	T1	700 µH/EE20	7508111334	Wurth Electronics	1
42	VAR1	Varistor, 0.3 W/320 V	ERZE07A511	Panasonic	1
43	ZD1	22 V/800 mW	BZD27C22P-E3-08	Vishay	1
44	PCB	66 mm x 33 mm (L x W), single layer, 1 oz., FR-4			1

8 Transformer specification

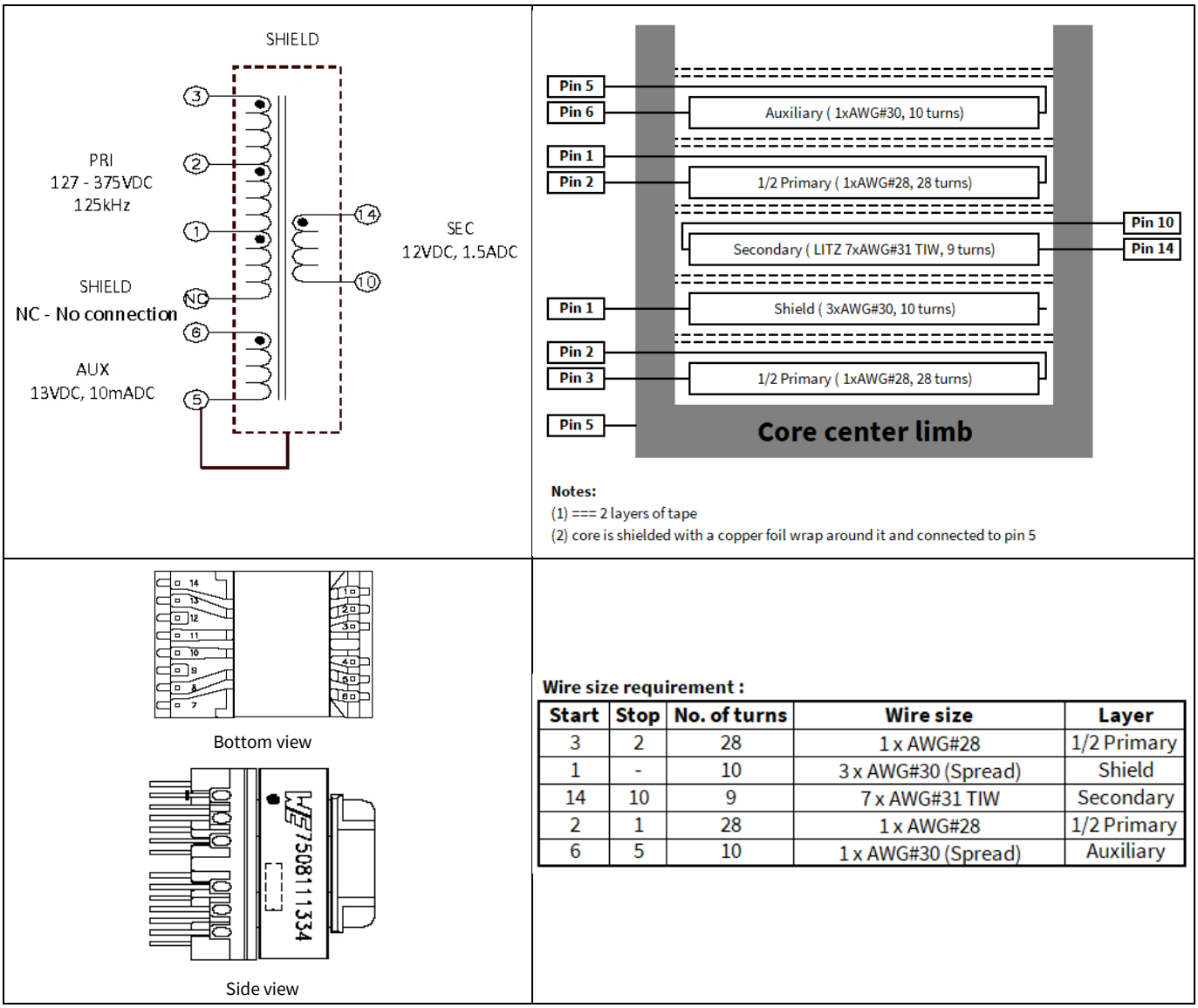
Refer to Appendix A for transformer design and Appendix B for WE transformer specification.

Wurth Electronics core part number: 150-1945 (EE20/10/6)

Wurth Electronics bobbin: 070-5643 (14-pin EXT, THT, horizontal version)

Primary inductance: L_P = 700 µH (±10 percent), measured between pin 1 and pin 3

Manufacturer and part number: Wurth Electronics Midcom (7508111334)



Wire size requirement :

Start	Stop	No. of turns	Wire size	Layer
3	2	28	1 x AWG#28	1/2 Primary
1	-	10	3 x AWG#30 (Spread)	Shield
14	10	9	7 x AWG#31 TIW	Secondary
2	1	28	1 x AWG#28	1/2 Primary
6	5	10	1 x AWG#30 (Spread)	Auxiliary

Figure 8 Transformer structure

9 Measurement data and graphs

Table 5 Electrical measurements

Input (V AC/Hz)	P_{IN} (W)	I_{OUT} (A)	V_{OUT} (V)		V_{RRP} (mV)	P_{OUT} (W)		Efficiency (%)		Average efficiency (%)		OLP P_{IN} (W)	OLP I_{OUT} (A)
			PCB	Cable	PCB	PCB	Cable	PCB	Cable	PCB	Cable		
90 V AC/ 60 Hz	0.034	0.000	12.164	12.164	66.04							28.40	2.00
	2.110	0.150	12.157	12.136	10.93	1.82	1.82	86.43%	86.28%				
	5.172	0.375	12.148	12.093	10.40	4.56	4.53	88.07%	87.67%	88.06%	87.06%		
	10.266	0.751	12.131	12.021	14.00	9.11	9.02	88.70%	87.89%				
	15.490	1.126	12.112	11.948	17.56	13.63	13.45	88.02%	86.82%				
	20.767	1.502	12.092	11.873	26.04	18.16	17.83	87.45%	85.86%				
115 V AC/ 60 Hz	0.034	0.000	12.163	12.163	65.16							30.34	2.17
	2.127	0.150	12.157	12.136	10.00	1.82	1.82	85.75%	85.60%				
	5.151	0.375	12.148	12.093	10.80	4.56	4.53	88.44%	88.04%	88.24%	87.24%		
	10.319	0.751	12.131	12.022	12.22	9.11	9.02	88.24%	87.45%				
	15.458	1.126	12.113	11.949	15.69	13.63	13.45	88.20%	87.01%				
	20.621	1.502	12.093	11.875	18.13	18.16	17.83	88.07%	86.48%				
230 V AC/ 50Hz	0.038	0.000	12.162	12.163	70.67							34.40	2.47
	2.221	0.150	12.158	12.136	76.00	1.82	1.82	82.10%	81.95%				
	5.246	0.375	12.148	12.093	10.40	4.56	4.53	86.84%	86.45%	87.57%	86.57%		
	10.381	0.751	12.131	12.022	13.38	9.11	9.02	87.71%	86.92%				
	15.509	1.126	12.114	11.950	14.31	13.64	13.45	87.92%	86.73%				
	20.693	1.502	12.096	11.876	18.13	18.17	17.84	87.79%	86.19%				
265 V AC/ 50 Hz	0.041	0.000	12.164	12.164	71.91							35.50	2.54
	2.260	0.150	12.157	12.135	76.93	1.82	1.82	80.69%	80.55%				
	5.351	0.375	12.146	12.093	10.84	4.55	4.53	85.12%	84.74%	87.06%	86.08%		
	10.436	0.751	12.130	12.021	12.76	9.10	9.02	87.25%	86.46%				
	15.498	1.126	12.113	11.950	14.58	13.63	13.45	87.98%	86.79%				
	20.665	1.502	12.095	11.878	18.89	18.16	17.84	87.90%	86.32%				

Note: Cable end testing done with 1.5 m long 0.5 mm 2x 2C wire.

100 percent load condition: 12 V/1.5 A

75 percent load condition: 12 V/1.125 A

50 percent load condition: 12 V/0.75 A

25 percent load condition: 12 V/0.375 A

10 percent load condition: 12 V/0.15 A

9.1 Efficiency curve

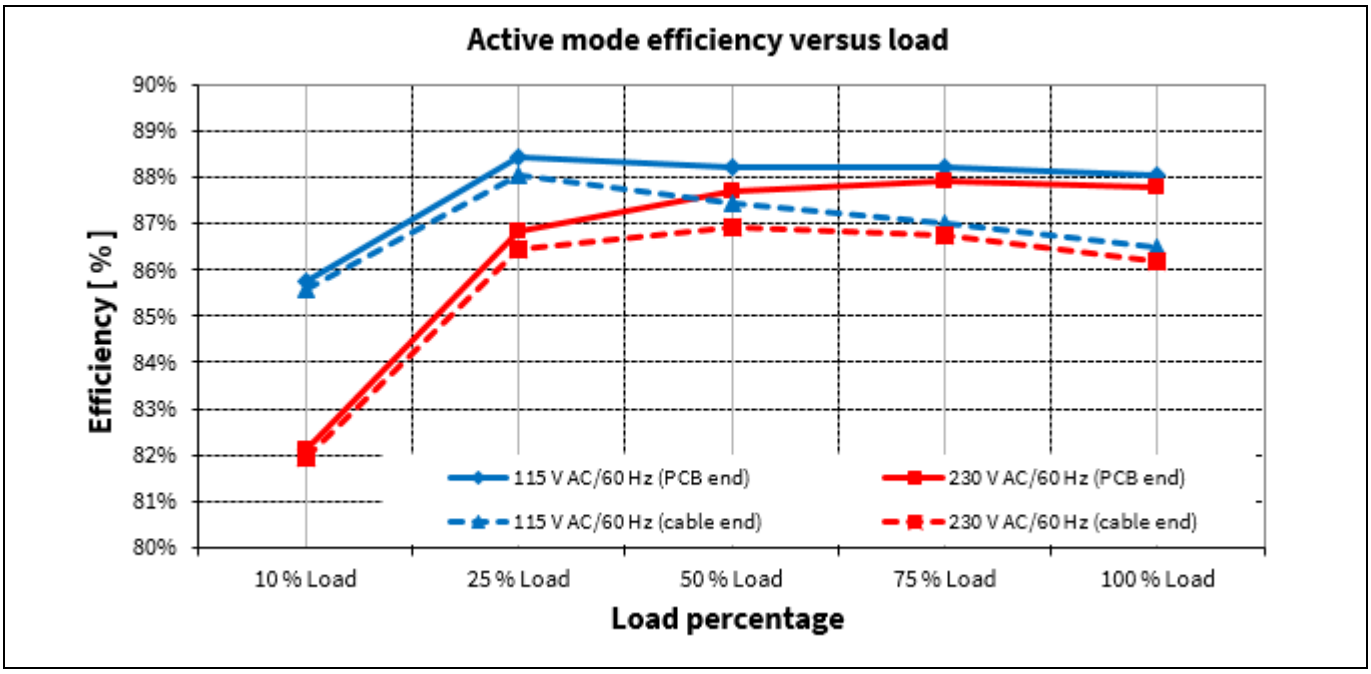


Figure 9 Efficiency vs output load (115 V AC and 230 V AC)

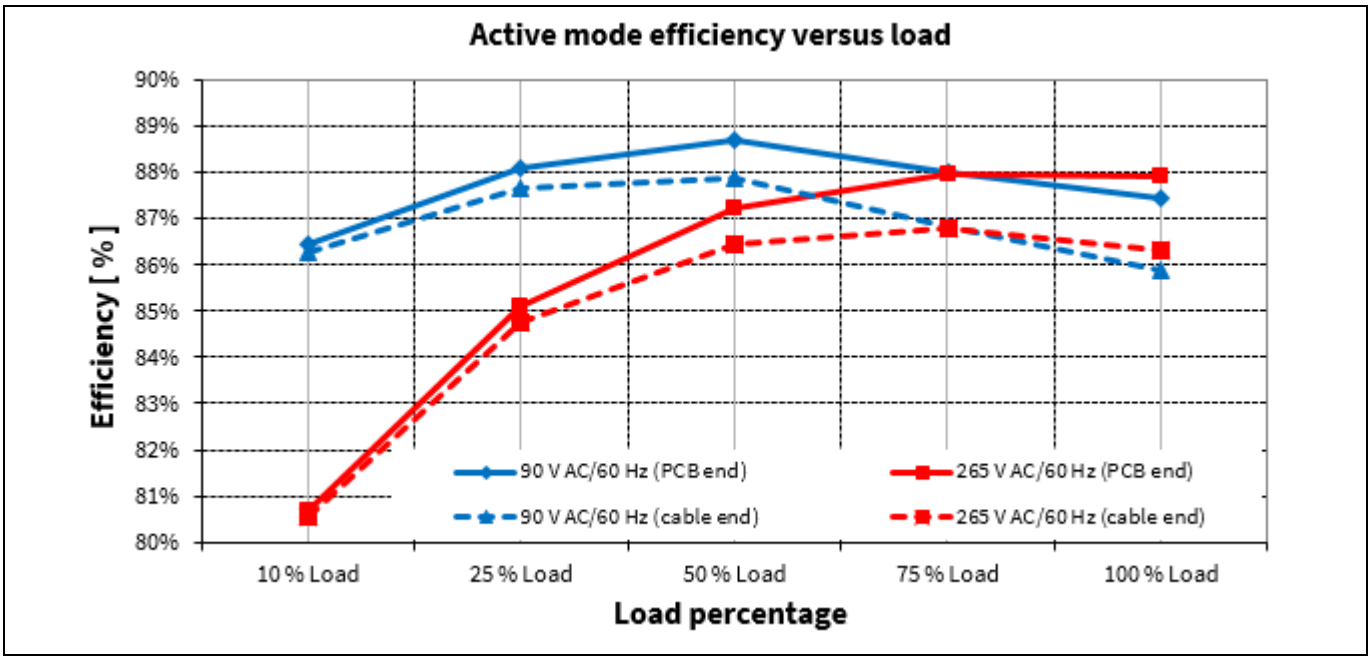


Figure 10 Efficiency vs output load (90 V AC and 265 V AC)

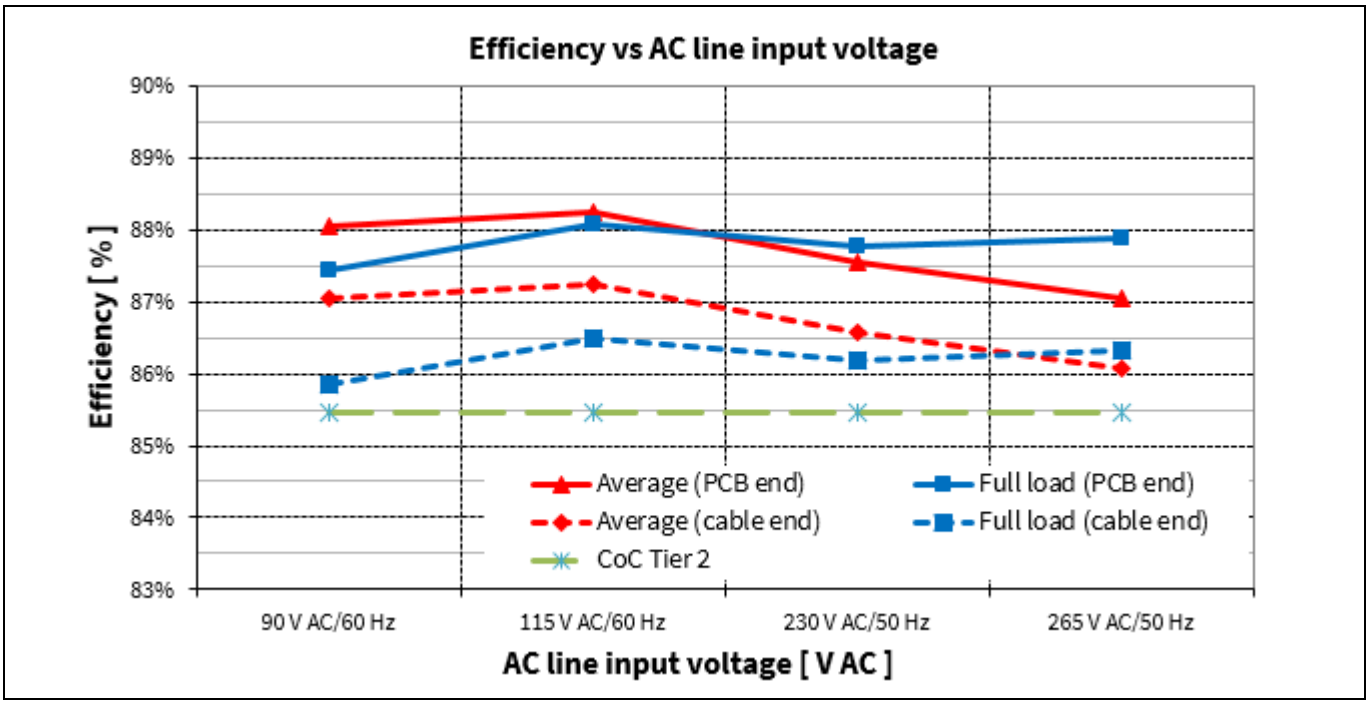


Figure 11 **Efficiency vs AC-line input voltage**

9.2 Standby power

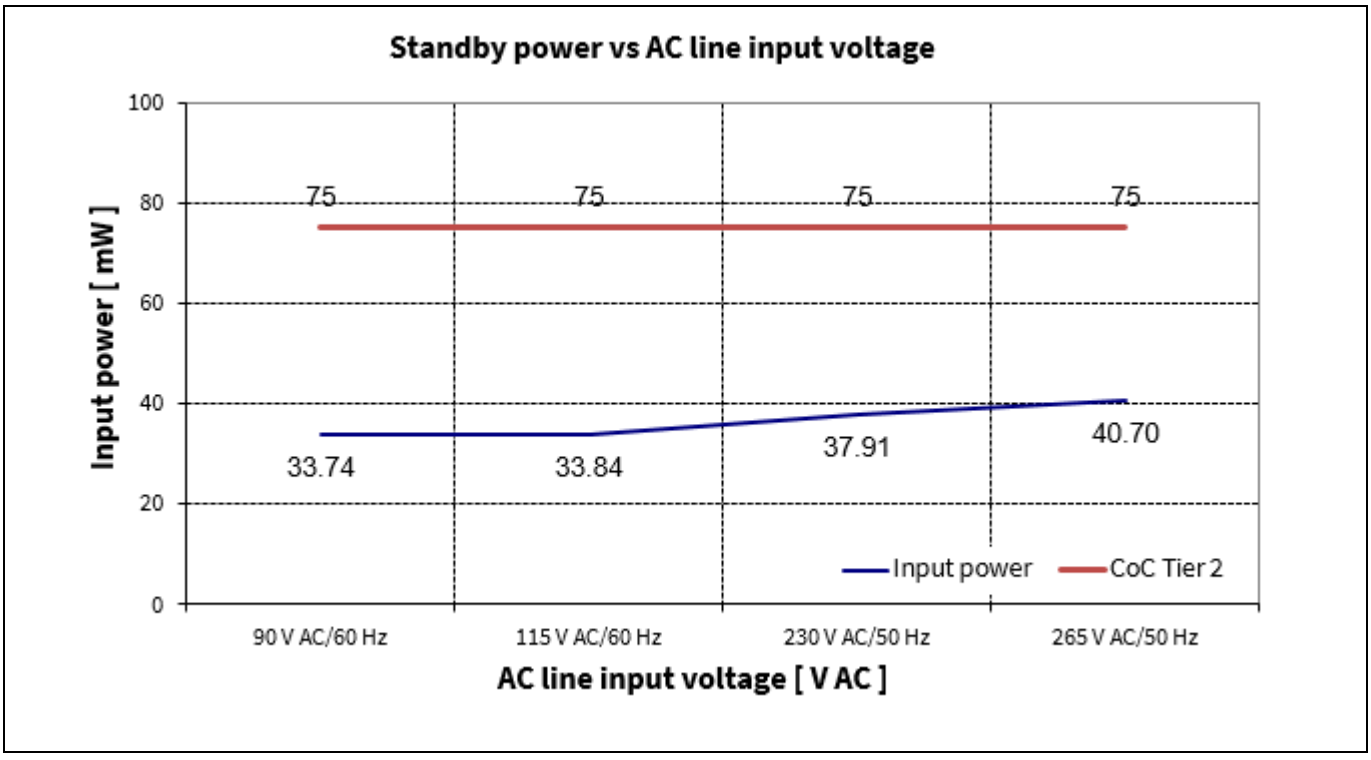


Figure 12 **Standby power at no load vs AC-line input voltage (measured by Yokogawa WT210 power meter – integration mode)**

9.3 Line and load regulation (PCB end)

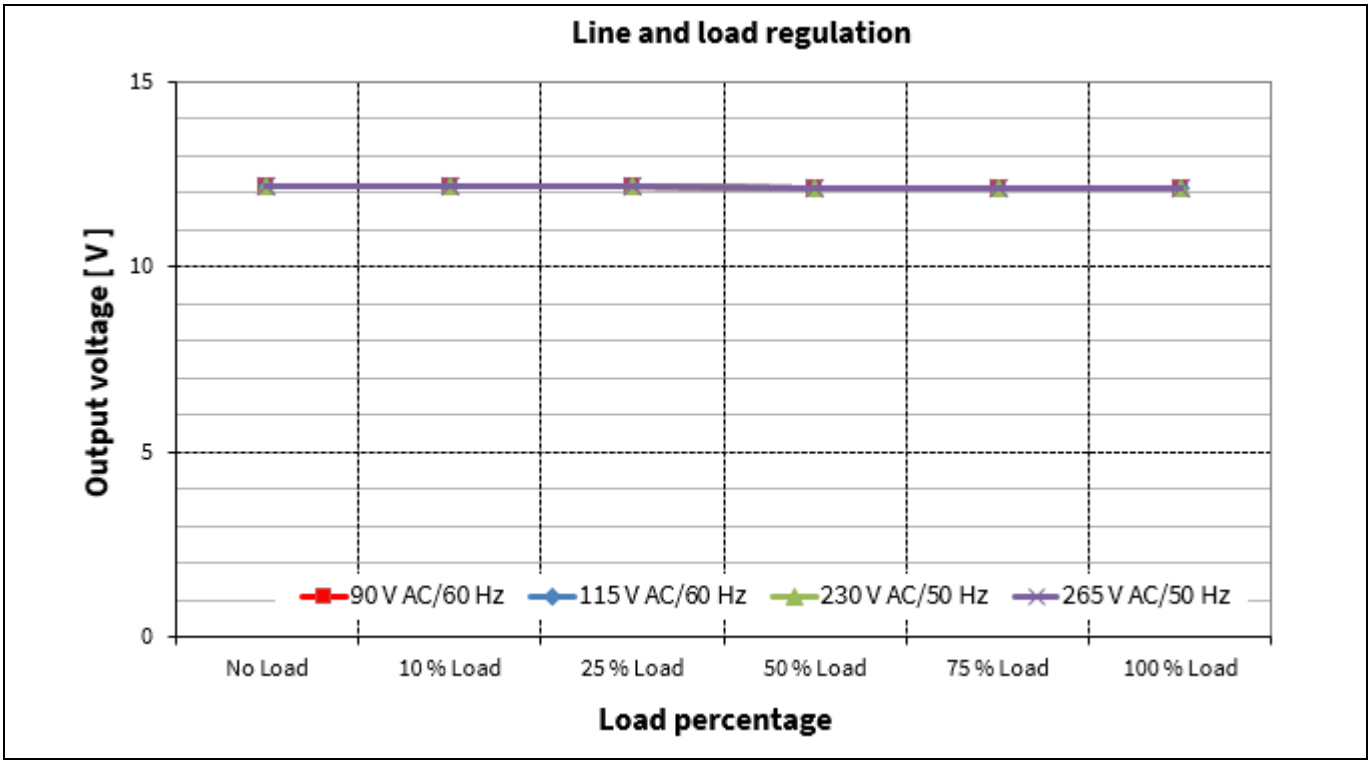


Figure 13 Output regulation vs load at different AC-line input voltage

9.4 Maximum input power

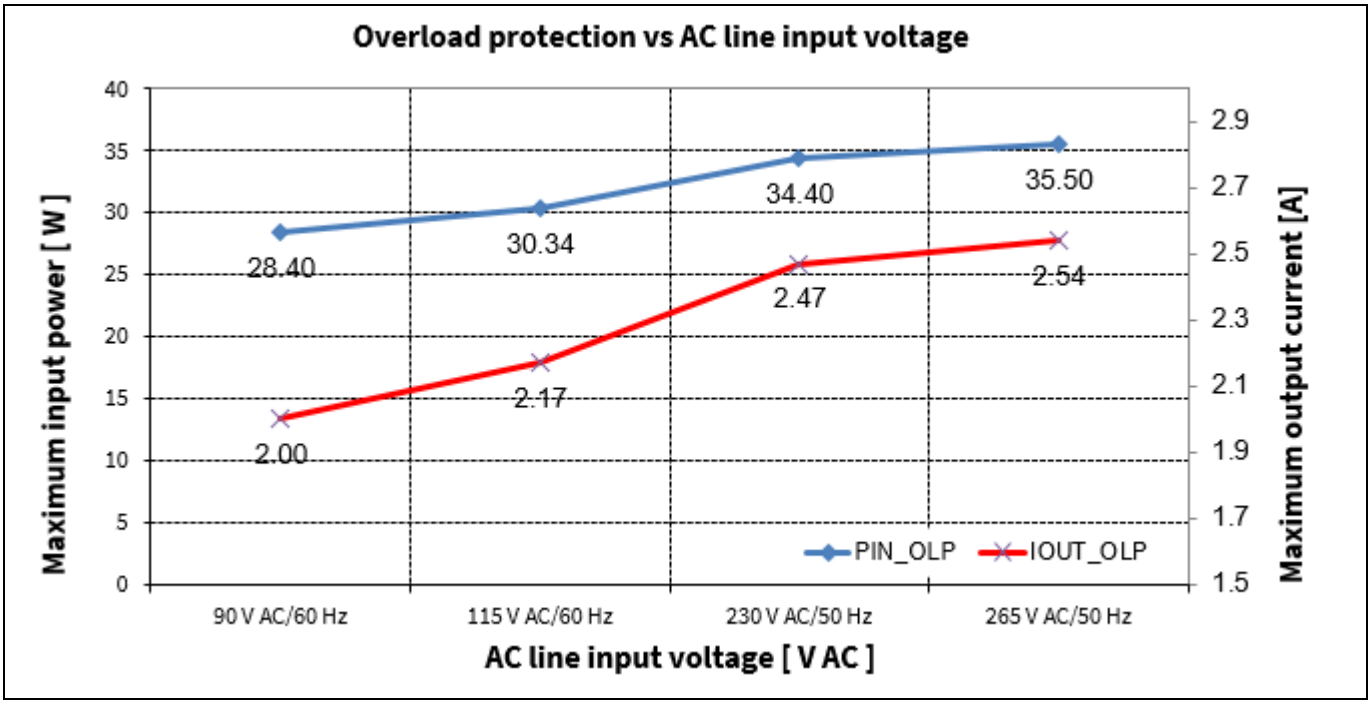


Figure 14 Maximum input power and output current (before over-load protection) vs AC-line input voltage

9.5 Frequency reduction

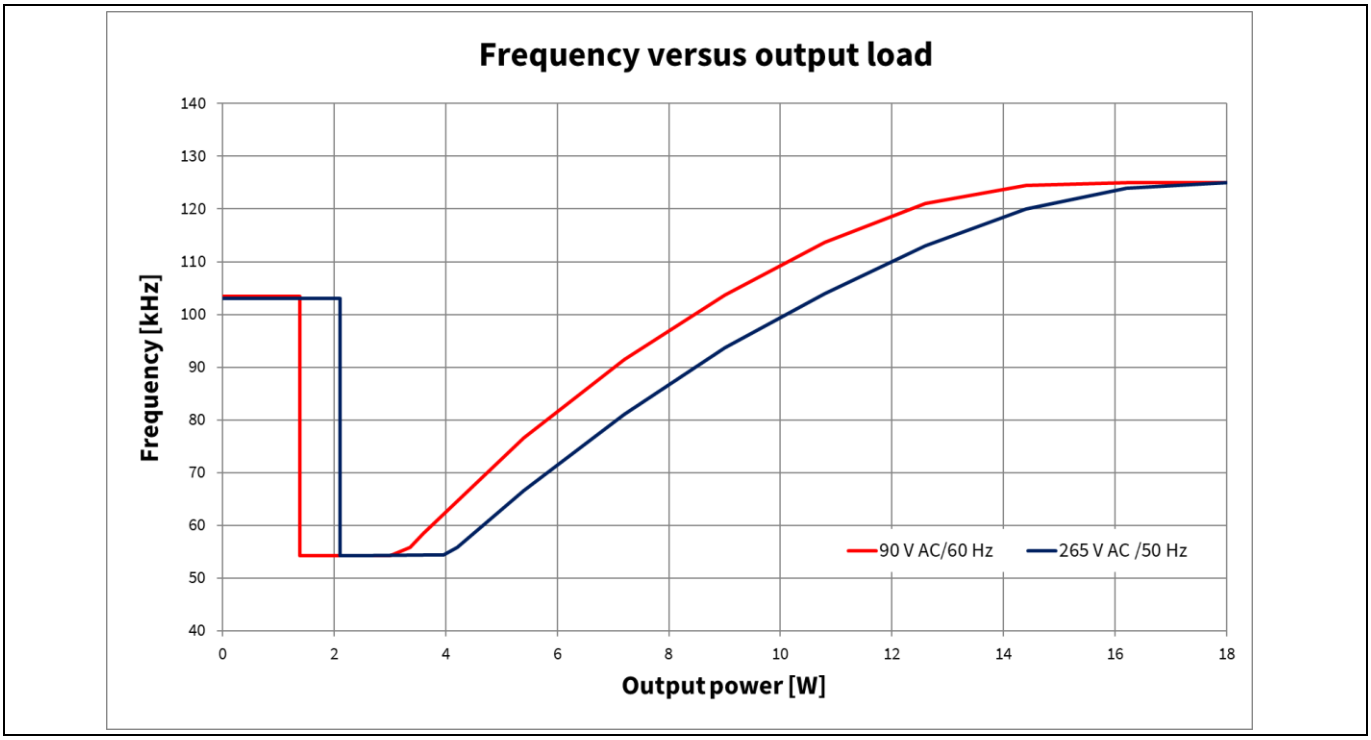


Figure 15 Frequency reduction curve vs output load

9.6 ESD immunity (EN 61000-4-2)

The reference board was subjected to a ±8 kV contact discharge and ±15 kV air discharge ESD test according to EN 61000-4-2. It was tested at full load (18 W) using resistive load (8 Ω) on the cable end at an input voltage of 115 V AC and 230 V AC. A test failure was defined as non-recoverable and/or system auto-restart.

- ±8 kV contact discharge: Pass
- ± 15 kV air discharge: Pass

Table 6 System ESD test result

Description	ESD test	Level	Number of strikes		Test result
			+12 V_{OUT}	GND	
115 V AC, 18 W (8 Ω R_{LOAD})	Contact	+8 kV	10	10	Pass
		-8 kV	10	10	Pass
	Air	+15 kV	10	10	Pass
		-15 kV	10	10	Pass
230 V AC, 18 W (8 Ω R_{LOAD})	Contact	+8 kV	10	10	Pass
		-8 kV	10	10	Pass
	Air	+15 kV	10	10	Pass
		-15 kV	10	10	Pass

9.7 Surge immunity (EN 61000-4-5)

The reference board was subjected to a surge immunity test (±1 kV DM and ±4 kV CM) according to EN 61000-4-5. It was tested at full load (18 W) using resistive load (8 Ω) on the cable end at an input voltage of 230 V AC. Output GND was connected to P.E. (protective earth) during testing. A test failure was defined as a non-recoverable and/or system auto-restart.

- ±1 kV DM: Pass
- ±4 kV CM: Pass

Table 7 System surge immunity test result

Description	Test	Level		Number of strikes				Test result
				0°	90°	180°	270°	
230 V AC, 18 W (8 Ω R_{LOAD})	DM	+1 kV	L → N	3	3	3	3	Pass
		-1 kV	L → N	3	3	3	3	Pass
	CM	+4 kV	L → GND	3	3	3	3	Pass
		+4 kV	N → GND	3	3	3	3	Pass
		-4 kV	L → GND	3	3	3	3	Pass
		-4 kV	N → GND	3	3	3	3	Pass

9.8 Conducted emissions (EN 55022 class B)

The conducted EMI was measured by Schaffner (SMR4503) and followed the test standard of EN 55022 (CISPR 22) class B. The reference board was tested at full load (18 W) using resistive load (8 Ω) on the cable end at an input voltage of 115 V AC and 230 V AC.

- 115 V AC: Pass with greater than 10 dB margin
- 230 V AC: Pass with greater than 10 dB margin

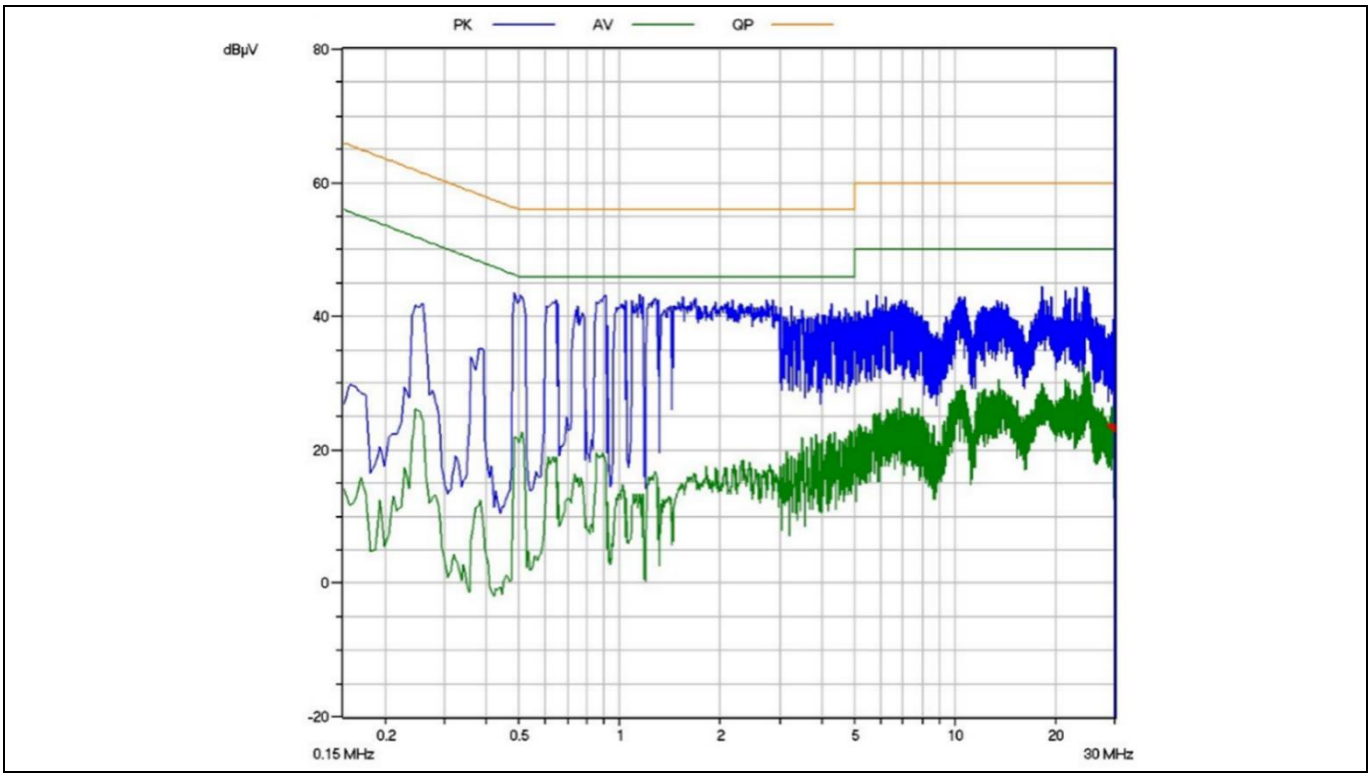


Figure 16 Conducted emissions (line) at 115 V AC and full load

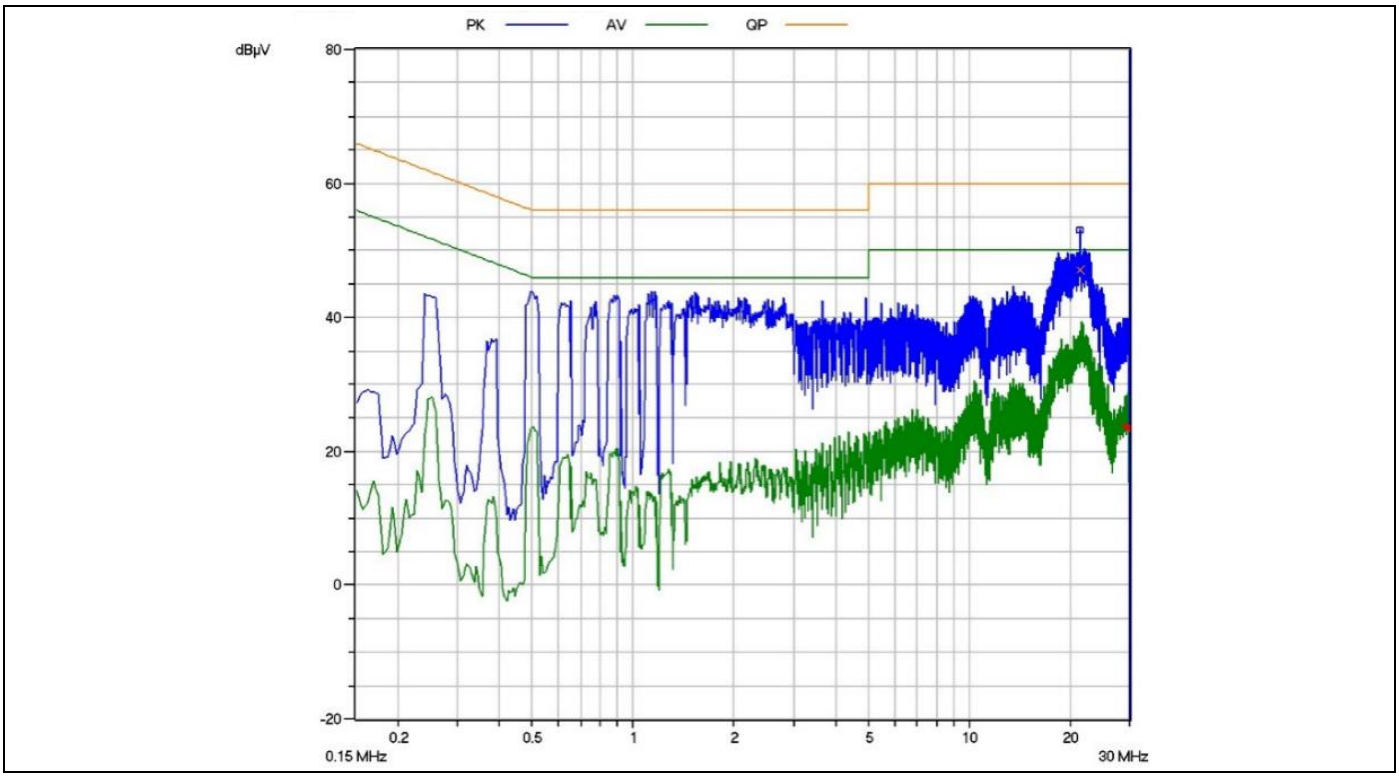


Figure 17 Conducted emissions (neutral) at 115 V AC and full load

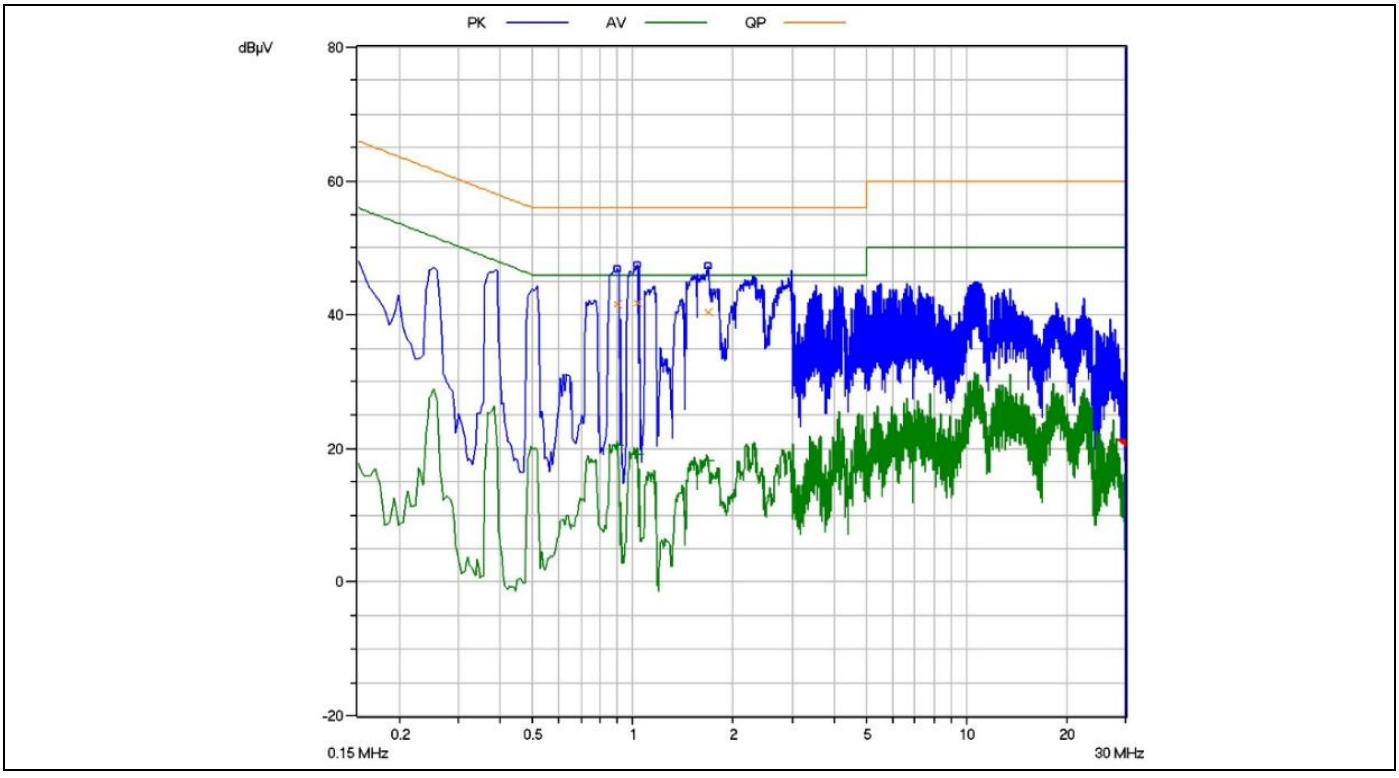


Figure 18 Conducted emissions (line) at 230 V AC and full load

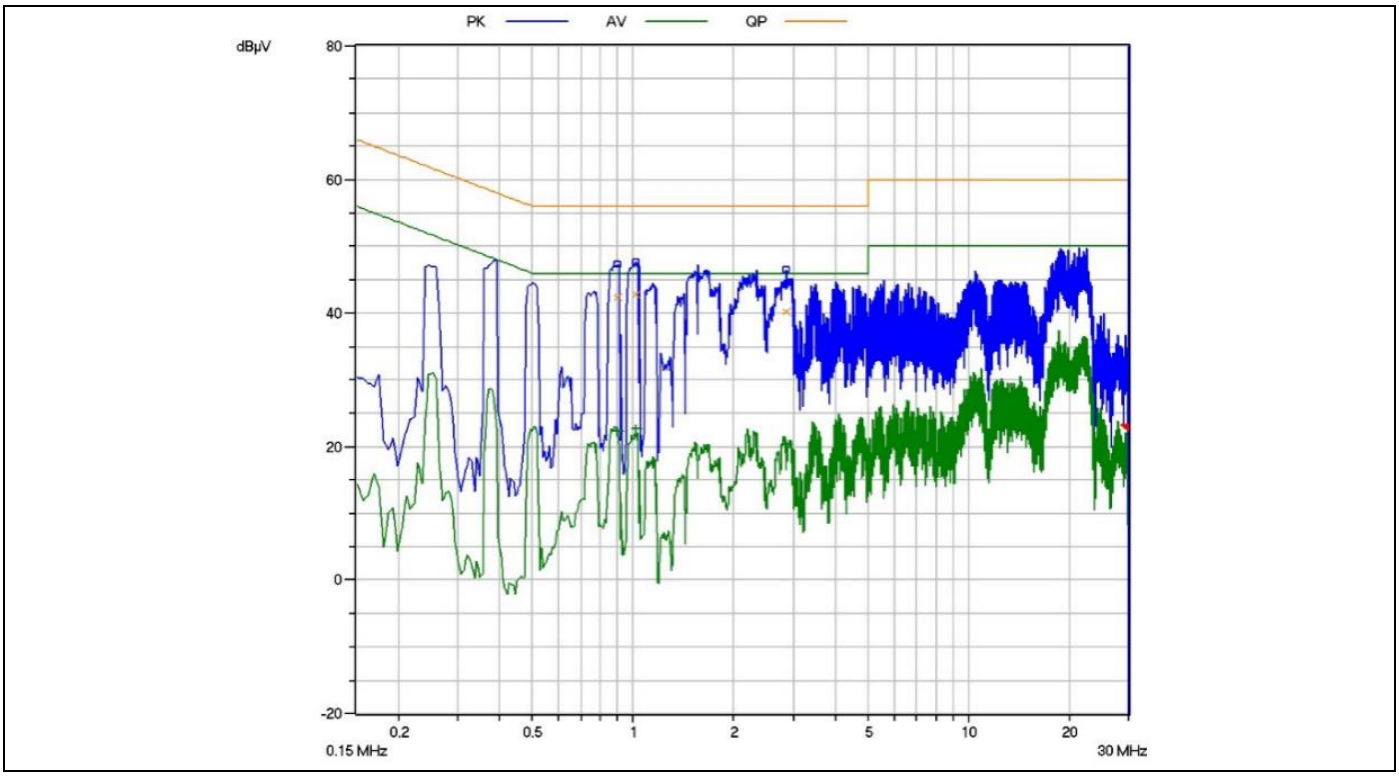


Figure 19 Conducted emissions (neutral) at 230 V AC and full load

9.9 Thermal measurement

Thermal measurement was done using an infrared thermography camera (FLIR-T62101) at an ambient temperature of 25°C taken after one hour running at full load. The temperature of the components was taken in an open-frame set-up. A thermal measurement on a plastic case enclosure (75 x 43 x 27 mm) with the unit placed inside was below 65°C and was also done for reference only (see Figure 22).

Table 8 Thermal measurement on components (open frame)

No.	Components	Temperature at 90 V AC (°C)	Temperature at 265 V AC (°C)
1	D4 (+12 V diode)	77.1	77.4
2	T1 (Transformer)	61.5	69.8
3	NTC1 (Thermistor)	57.1	43.0
4	Q1 (IPN70R1K2P7S)	71.6	86.4
5	IC1 (ICE5GSAG)	56.7	59.4
6	BR1 (Diode bridge)	58.7	41.4

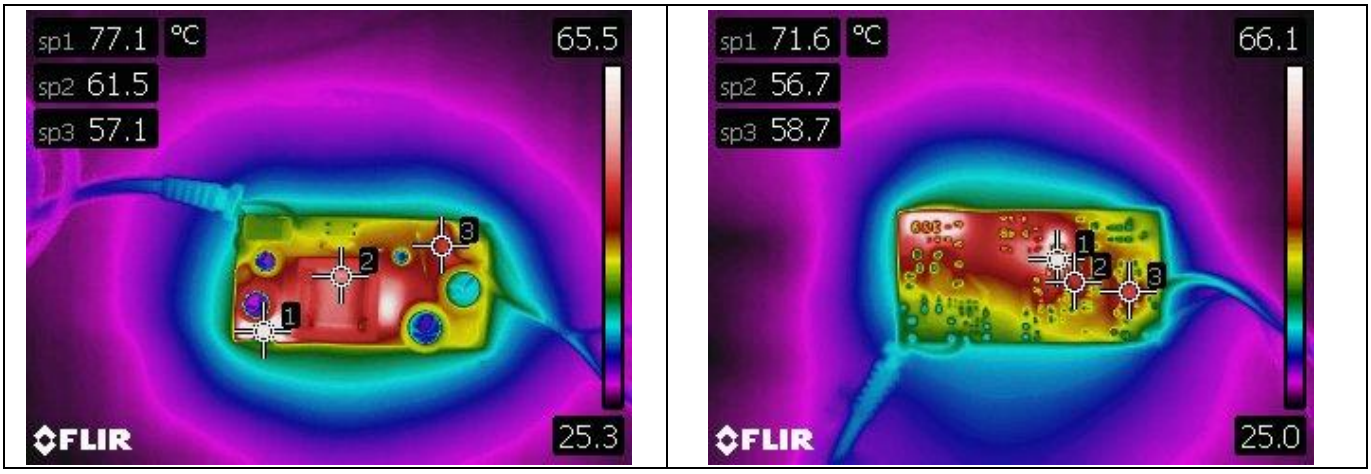


Figure 20 Top layer (left) and bottom layer (right) thermal image at 90 V AC input voltage

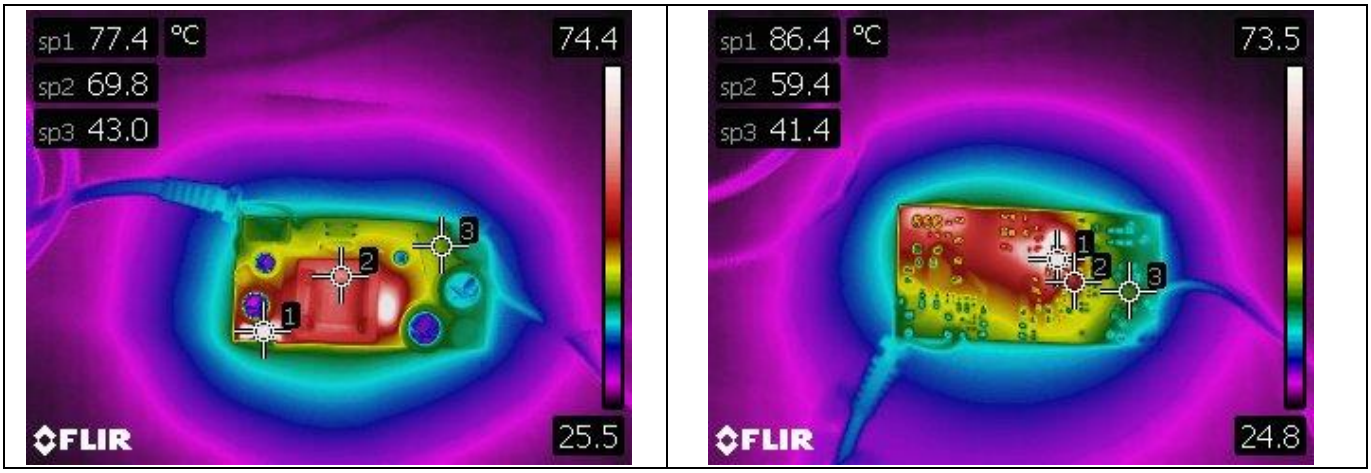


Figure 21 Top layer (left) and bottom layer (right) thermal image at 265 V AC input voltage

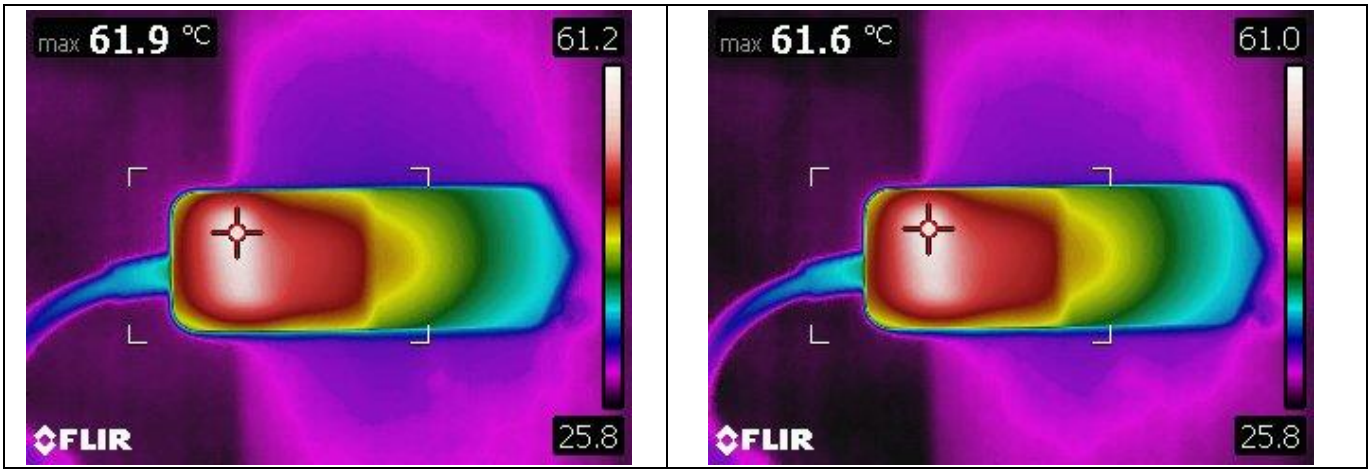


Figure 22 Plastic case thermal image at 90 V AC (left) and 265 V AC (right) input voltage

10 Waveforms and oscilloscope plots

All waveforms and scope plots were recorded with a Teledyne LeCroy HDO4034 oscilloscope.

10.1 Start-up at full load

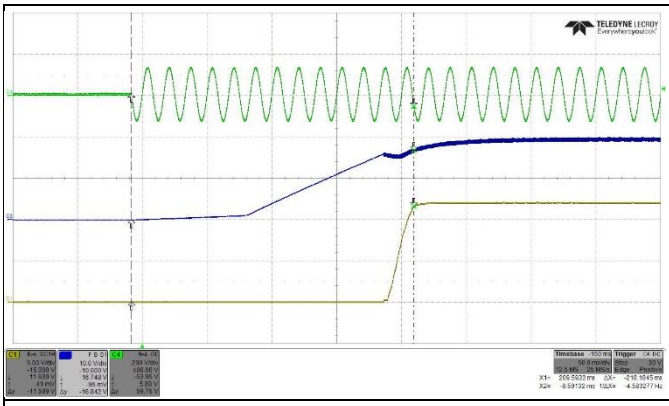
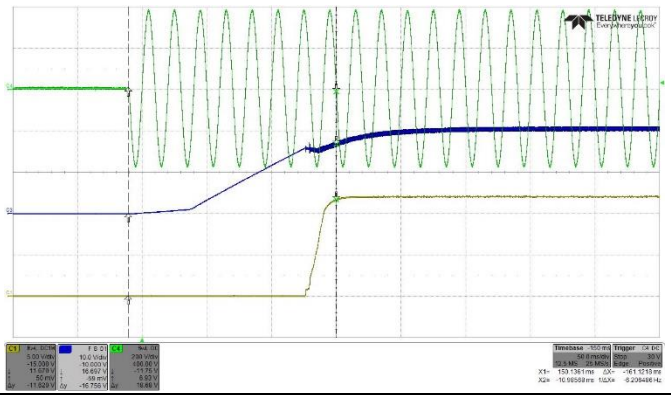
	
C1 (yellow) : +12 V output voltage C3 (blue) : V_{CC} voltage C4 (green) : AC-line voltage	C1 (yellow) : +12 V output voltage C3 (blue) : V_{CC} voltage C4 (green) : AC-line voltage
90 V AC start-up time at full load is less than 220 ms	265 V AC start-up time at full load is less than 170 ms

Figure 23 Start-up

10.2 Soft-start at full load

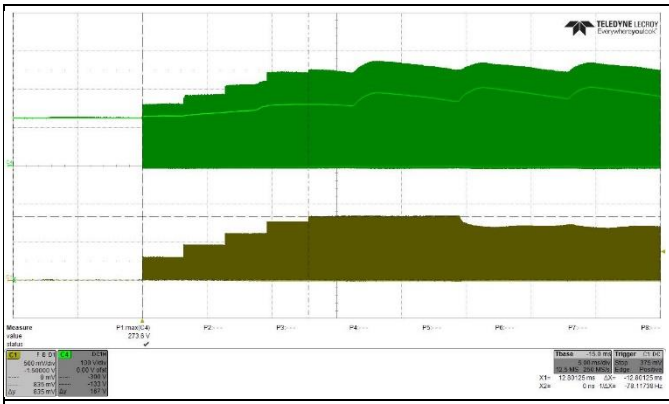
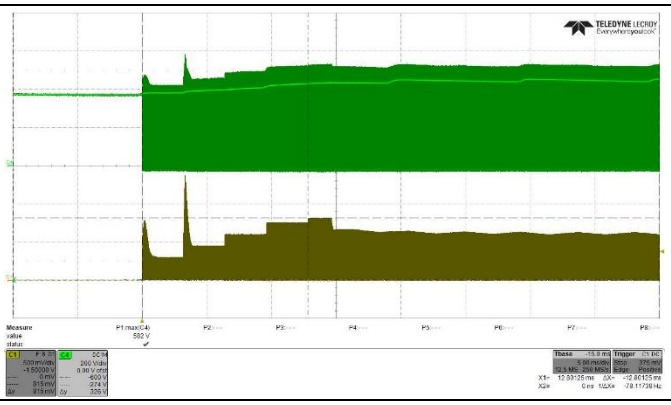
	
C1 (yellow) : CS voltage C4 (green) : Drain voltage	C1 (yellow) : CS voltage C4 (green) : Drain voltage
90 V AC soft-start time at full load is ~13 ms	265 V AC soft-start time at full load is ~13 ms

Figure 24 Soft-start

10.3 Drain and CS voltage at full load

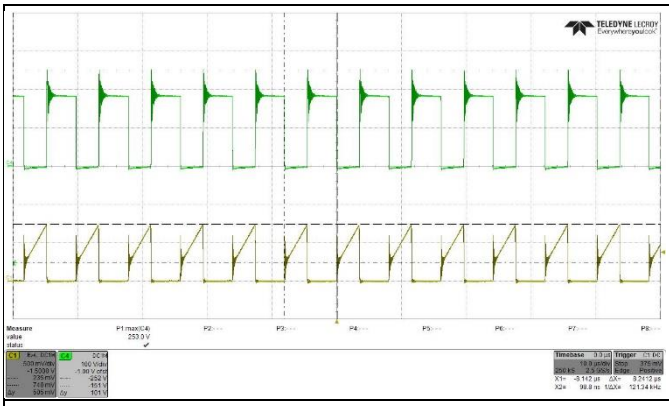
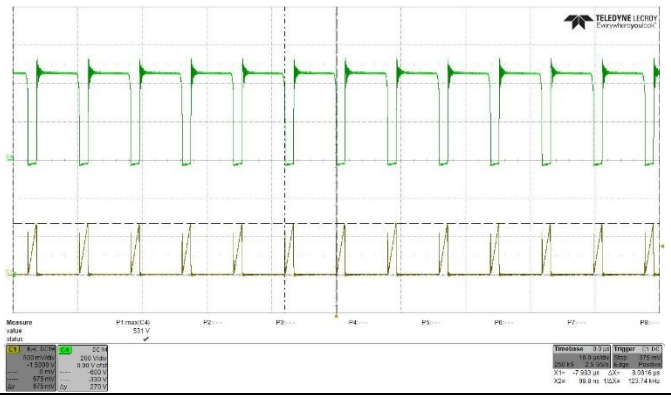
	
C1 (yellow) : CS voltage C4 (green) : Drain voltage	C1 (yellow) : CS voltage C4 (green) : Drain voltage
90 V AC maximum drain voltage at full load is ~253 V	265 V AC maximum drain voltage at full load is ~531 V

Figure 25 Drain and CS voltage

10.4 Frequency jittering at full load

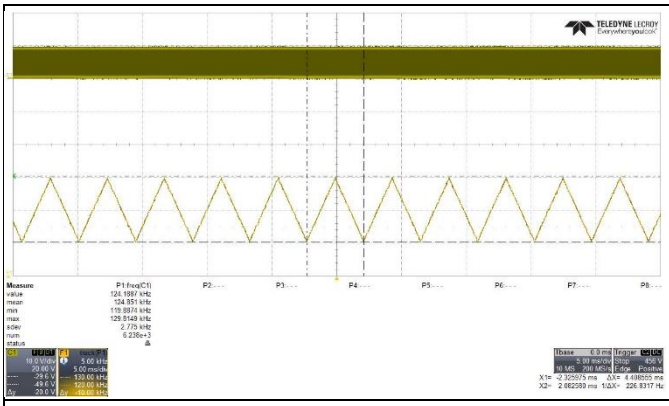
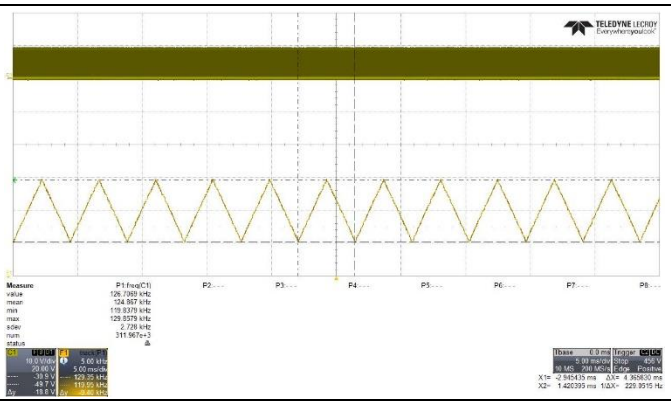
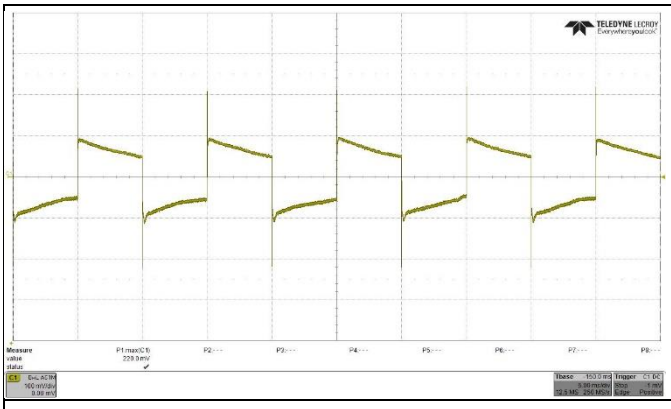
	
C1 (yellow) : Gate voltage F1 (yellow) : Frequency track of gate voltage	C1 (yellow) : Gate voltage F1 (yellow) : Frequency track of gate voltage
90 V AC frequency jittering at full load is ~120 kHz to ~130 kHz with a jitter period of 4.4 ms	265 V AC frequency jittering at full load is ~120 kHz to ~130k Hz with a jitter period of 4.4 ms

Figure 26 Frequency jittering

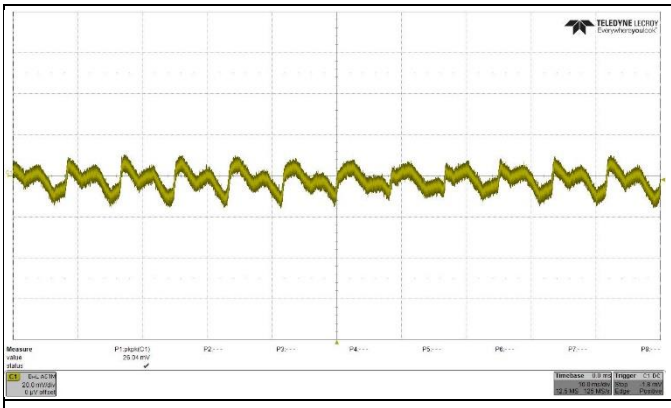
10.5 Load transient response (dynamic load from 10 percent to 100 percent)



C1 (yellow) : +12 V output voltage	C1 (yellow) : +12 V output voltage
90 V AC +12 V output voltage $V_{ripple\_pk\_pk}$ is ~220 mV	265 V AC +12 V output voltage $V_{ripple\_pk\_pk}$ is ~225 mV

Figure 27 Load transient response with +12 V output load change from 10 percent to 100 percent at 0.4 A/µs slew rate, 100 Hz. Probe terminals are connected on the PCB end and decoupled with a 1 µF electrolytic and 0.1 µF ceramic capacitor. Oscilloscope is bandwidth filter limited to 20 MHz.

10.6 Output ripple voltage at full load



C1 (yellow) : +12 V output voltage	C1 (yellow) : +12 V output voltage
90 V AC +12 V output voltage $V_{ripple\_pk\_pk}$ is ~26 mV	265 V AC +12 V output voltage $V_{ripple\_pk\_pk}$ is ~19 mV

Figure 28 Output ripple voltage at full load. Probe terminals are connected on the PCB end and decoupled with a 1 µF electrolytic and 0.1 µF ceramic capacitor. Oscilloscope is bandwidth filter limited to 20 MHz.

10.7 Output ripple voltage at ABM (10 mA load)

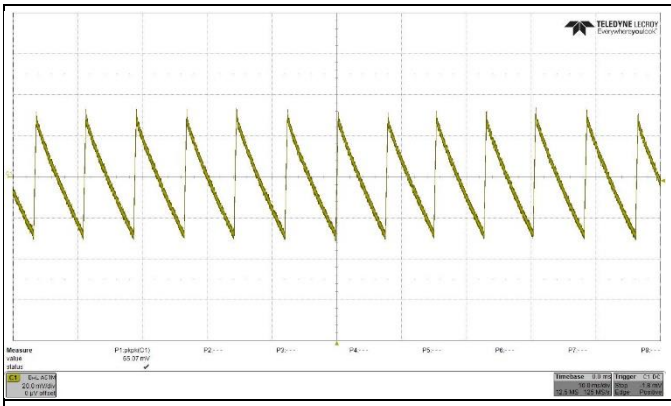
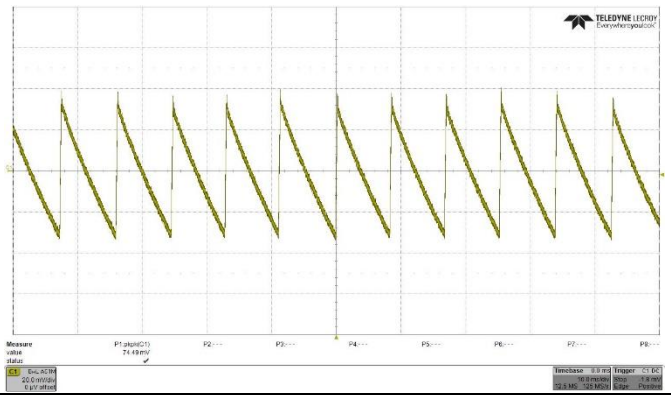
	
C1 (yellow) : +12 V output voltage	C1 (yellow) : +12 V output voltage
90 V AC +12 V output voltage $V_{ripple\_pk\_pk}$ is ~65 mV	265 V AC +12 V output voltage $V_{ripple\_pk\_pk}$ is ~75 mV

Figure 29 Output ripple voltage at 10 mA load. Probe terminals are connected on the PCB end and decoupled with a 1 µF electrolytic and 0.1 µF ceramic capacitor. Oscilloscope is bandwidth filter limited to 20 MHz.

10.8 Entering ABM

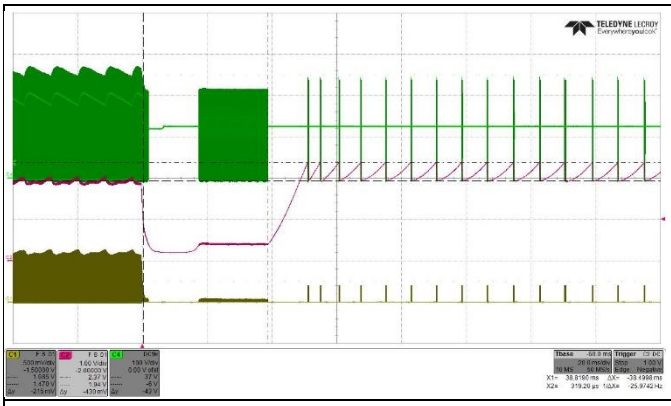
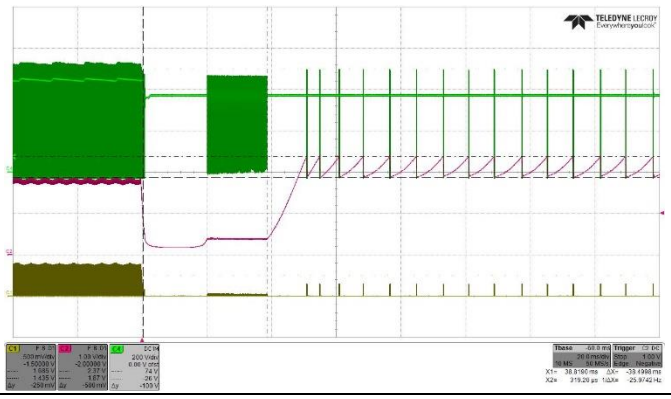
	
C1 (yellow) : CS voltage C2 (purple) : FB pin voltage C4 (green) : Drain voltage	C1 (yellow) : CS voltage C2 (purple) : FB pin voltage C4 (green) : Drain voltage
90 V AC full load to 10 mA load. Enter ABM at FB pin voltage less than 1.03 V (V_{FB_EBHP}) for more than 36 ms (t_{FB_BEB}).	265 V AC full load to 10 mA load. Enter ABM at FB pin voltage less than 1.03 V (V_{FB_EBHP}) for more than 36 ms (t_{FB_BEB}).

Figure 30 Entering ABM. Output at full load to 10 mA load.

10.9 During ABM

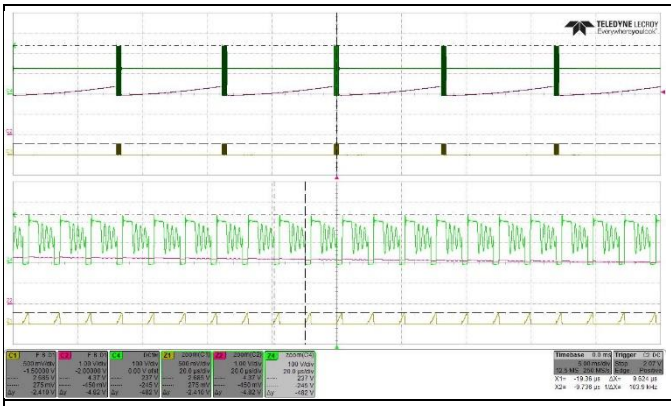
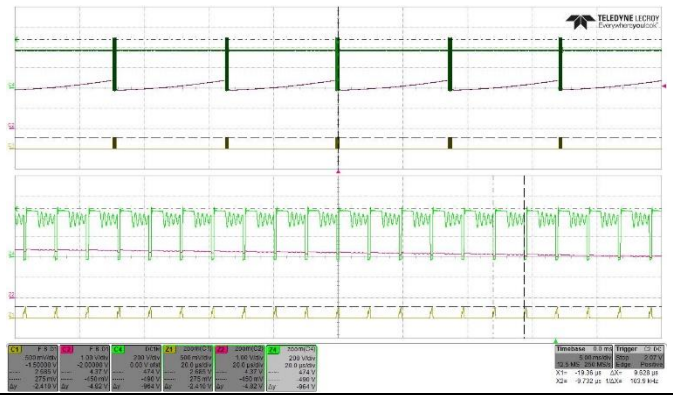
	
C1 (yellow) : CS voltage C2 (purple) : FB pin voltage C4 (green) : Drain voltage	C1 (yellow) : CS voltage C2 (purple) : FB pin voltage C4 (green) : Drain voltage
90 V AC at 10 mA load. Burst-on at FB voltage 2.35 V ($V_{FB\_Bon\_NISO}$) and burst-off at 2 V ($V_{FB\_BOff\_NISO}$). CS voltage at 0.27 V (V_{CS_BHP}). Switching frequency at 104 kHz (f_{OSC2_ABM}).	265 V AC at 10 mA load. Burst-on at FB voltage 2.35 V ($V_{FB\_Bon\_NISO}$) and burst-off at 2 V ($V_{FB\_BOff\_NISO}$). CS voltage at 0.27 V (V_{CS_BHP}). Switching frequency at 104 kHz (f_{OSC2_ABM}).

Figure 31 During ABM. Output at 10 mA load.

10.10 Leaving ABM

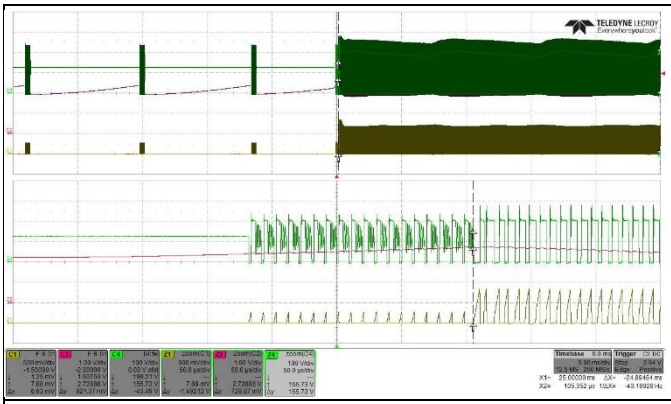
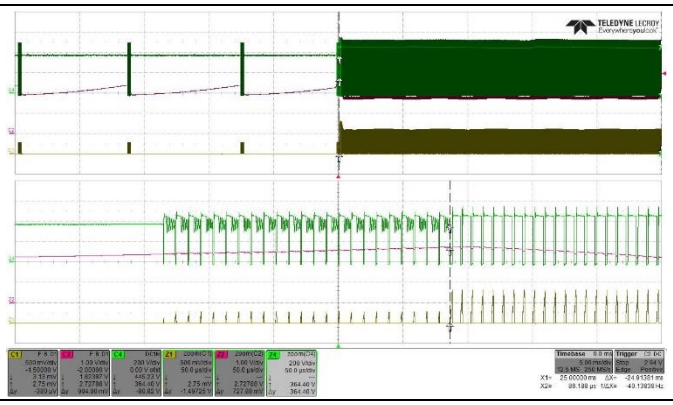
	
C1 (yellow) : CS voltage C2 (purple) : FB pin voltage C4 (green) : Drain voltage	C1 (yellow) : CS voltage C2 (purple) : FB pin voltage C4 (green) : Drain voltage
90 V AC at 10 mA load to full load. Leave ABM at FB voltage greater than 2.73 V (V_{FB_LB}).	265 V AC at 10 mA load to full load. Leave ABM at FB voltage greater than 2.73 V (V_{FB_LB}).

Figure 32 Leaving ABM. Output at 10 mA load to full load.

10.11 V_{CC} OV/UV protection

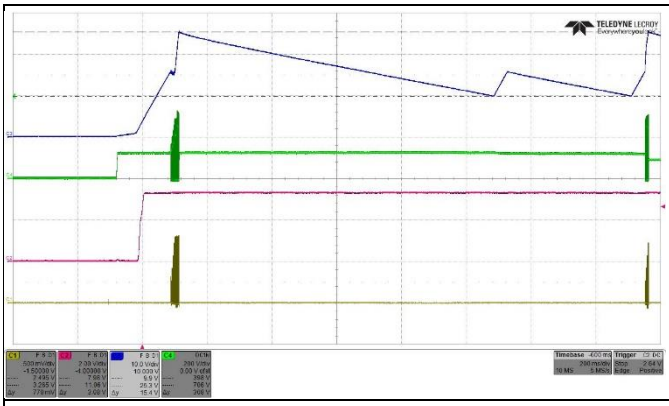
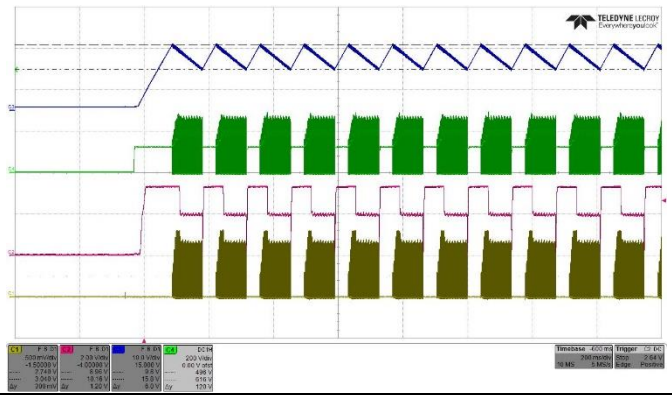
	
C1 (yellow) : CS voltage C2 (purple) : FB pin voltage C3 (blue) : V_{CC} voltage C4 (green) : Drain voltage	C1 (yellow) : CS voltage C2 (purple) : FB pin voltage C3 (blue) : V_{CC} voltage C4 (green) : Drain voltage
90 V AC at no load. Removed R10 and R15. Trigger V_{CC} OV protection at V_{CC} voltage greater than 25.5 V (V_{VCC_OVP}). Odd-skip auto-restart mode.	90 V AC at full load. Removed R9. Trigger V_{CC} UV protection at V_{CC} voltage less than 10 V (V_{VCC_OFF}). Auto-restart mode.

Figure 33 V_{CC} OV/UV protection

10.12 Over-load protection

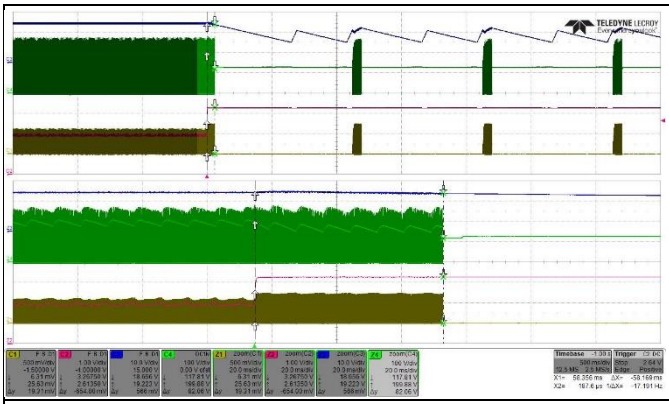
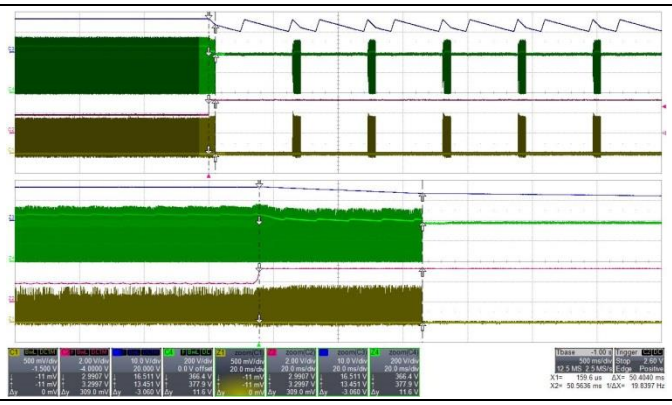
	
C1 (yellow) : CS voltage C2 (purple) : FB pin voltage C3 (blue) : V_{CC} voltage C4 (green) : Drain voltage	C1 (yellow) : CS voltage C2 (purple) : FB pin voltage C3 (blue) : V_{CC} voltage C4 (green) : Drain voltage
90 V AC at full load to over-load. Trigger protection at FB pin voltage greater than 2.73 V (V_{FB_OLP}) for more than 54 ms ($t_{FB\_OLP\_B}$). Odd-skip auto-restart mode.	265 V AC at full load to over-load. Trigger protection at FB pin voltage greater than 2.73 V (V_{FB_OLP}) for more than 54 ms ($t_{FB\_OLP\_B}$). Odd-skip auto-restart mode.

Figure 34 Over-load protection. Load increased from full load to 2.5 A load to trigger protection.

10.13 Hold-up time

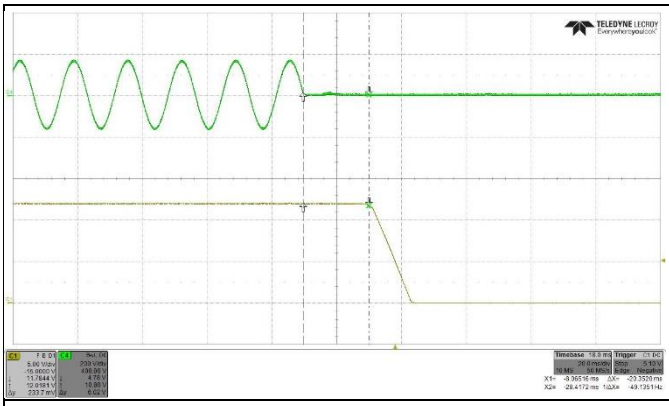
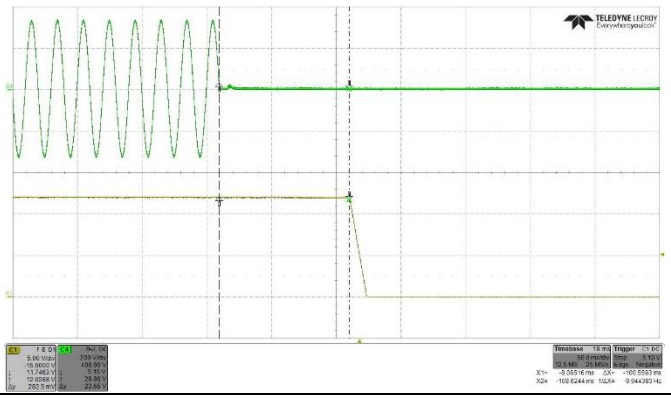
	
C1 (yellow) : +12 V output voltage C4 (green) : AC-line voltage	C1 (yellow) : +12 V output voltage C4 (green) : AC-line voltage
115 V AC full-load hold-up time is 20.3 ms	230 V AC full-load hold-up time is 100 ms

Figure 35 Hold-up time at full load

10.14 In-rush current

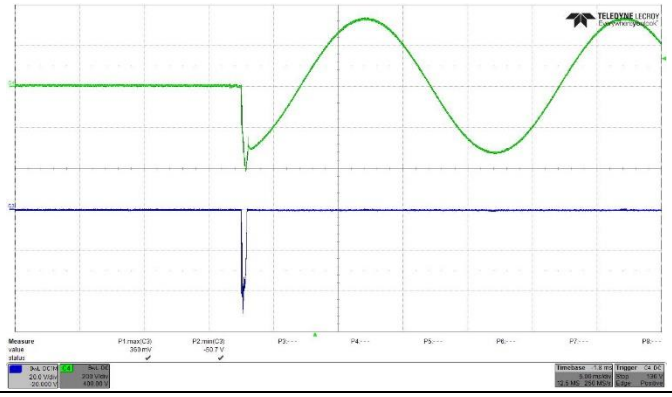

C3 (Blue) : AC-line current C4 (Green) : AC-line voltage
230 V AC in-rush current ~50 A

Figure 36 In-rush current at 230 V AC cold start-up with 25°C ambient temperature

11 Appendix A: Transformer design and spreadsheet [4]

Calculation tool for FF flyback converter using fifth-generation CoolSET™ (version 1.0)

Project:	90 ~ 265 V AC 18 W isolated flyback
Application:	Adapter for set-top box
CoolSET™:	ICE5GSAG
Date:	24 July 2018
Revision:	V 1.0

Notes:
Enter design variables in yellow-colored cells
Read design results in green-colored cells
Equation numbers are according to the Design Guide.
Select component values based on standard values available.
Voltage/current rating does not include design margin, voltage spikes and transient currents.
In "Output regulation", only fill in either isolated or non-isolated, whichever is applicable.

	Description	Eq #	Parameter	Unit	Value
Input, output, CoolSET™ specs					
Line input					
Input	Minimum AC input voltage		V_{ACMin}	[V]	90
Input	Maximum AC input voltage		V_{ACMax}	[V]	265
Input	Line frequency		f_{AC}	[Hz]	60
Input	Bus capacitor DC ripple voltage		$V_{DCRipple}$	[V]	27
Output 1 specs					
Input	Output voltage 1		V_{Out1}	[V]	12
Input	Output current 1		I_{Out1}	[A]	1.50
Input	Forward voltage of output diode 1		V_{FOut1}	[V]	0.4
Input	Output ripple voltage 1		$V_{OutRipple1}$	[V]	0.1
Result	Output power 1	Eq 001	P_{Out1}	[W]	18
Auxiliary					
Input	V_{CC} voltage		V_{Vcc}	[V]	13
Input	Forward voltage of V_{CC} diode (D2)		$V_{F\,Vcc}$	[V]	0.6
Power					
Input	Efficiency		η		0.88
Result	Nominal output power	Eq 003	P_{OutNom}	[W]	18.00
Input	Maximum output power for over-load protection		P_{OutMax}	[W]	18
Result	Maximum input power for over-load protection	Eq 006	P_{InMax}	[W]	20.45
Input	Minimum output power		P_{OutMin}	[W]	2
Controller/CoolSET™					
	Controller/ CoolSET™				ICE5GSAG
Input	Switching frequency		f_S	[Hz]	125000
Input	Targeted max. drain-source voltage		V_{DSMax}	[V]	700
Input	Max. ambient temperature		T_{amax}	[°C]	40
Diode bridge and input capacitor					
Diode bridge					
Input	Power factor		cosφ		0.5
Result	Maximum AC input current	Eq 007	I_{ACRMS}	[A]	0.455
Result	Peak voltage at V_{ACMax}	Eq 008	$V_{DCMaxPk}$	[V]	374.77

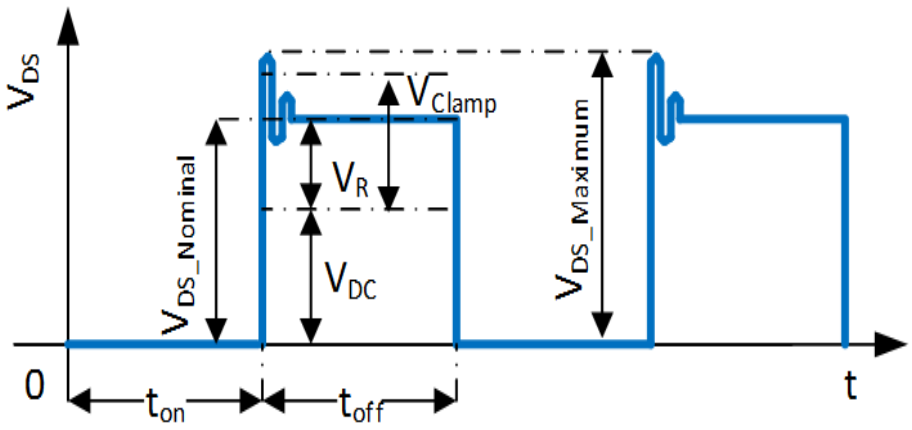
Appendix A: Transformer design and spreadsheet [4]

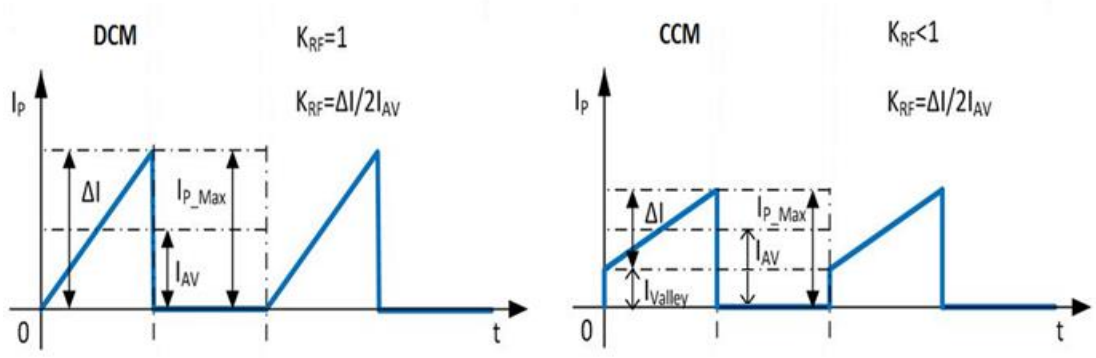
Input capacitor

Result	Peak voltage at V_{ACMin}	Eq 009	$V_{DCMinPk}$	[V]	127.28
Result	Selected minimum DC input voltage	Eq 010	$V_{DCMinSet}$	[V]	100.28
Result	Discharging time at each half-line cycle	Eq 011	T_D	[ms]	6.57
Result	Required energy at discharging time of input capacitor	Eq 012	W_{In}	[Ws]	0.13
Result	Calculated input capacitor	Eq 013	C_{INCal}	[µF]	43.77
Input	Select input capacitor (C1)		C_{in}	[µF]	44
Result	Calculated minimum DC input voltage	Eq 015	V_{DCMin}	[V]	100.44

Transformer design

Drain voltage and current waveform





Primary inductance and winding currents

Input	Reflection voltage		V_{RSET}	[V]	77
Result	Maximum duty cycle	Eq 016	D_{Max}		0.43
Input	Select current ripple factor		K_{RF}		0.53
Result	Primary inductance	Eq 017	L_P	[H]	7.01E-04
Result	Primary turn-on average current	Eq 018	I_{AV}	[A]	0.47
Result	Primary peak-to-peak current	Eq 019	ΔI	[A]	0.50
Result	Primary peak current	Eq 020	I_{PMax}	[A]	0.72
Result	Primary valley current	Eq 021	I_{Valley}	[A]	0.22
Result	Primary RMS current	Eq 022	I_{PRMS}	[A]	0.323

Appendix A: Transformer design and spreadsheet [4]

Select core type

Input	Select core type				1
Result	Core type				EE20/10/6
Result	Core material				TP4A(TDG)
Result	Maximum flux density		B_{Max}	[T]	0.3
Result	Cross-sectional area		A_e	[mm²]	32
Result	Bobbin width		BW	[mm]	11
Result	Winding cross-section		A_N	[mm²]	34
Result	Average length of turn		l_N	[mm]	41.2

Winding calculation

Result	Calculated minimum number of primary turns	Eq 023	N_{PCal}	Turns	52.43
Input	Select number of primary turns		N_P	Turns	56
Result	Calculated number of secondary 1 turns	Eq 024	N_{S1Cal}	Turns	9.02
Input	Select number of secondary 1 turns		N_{S1}	Turns	9
Result	Calculated number of auxiliary turns	Eq 026	N_{VccCal}	Turns	9.87
Input	Select number of auxiliary turns		N_{Vcc}	Turns	10
Result	Calculated V_{CC} voltage	Eq 027	V_{VccCal}	[V]	13.18

Post calculation

Result	Primary to secondary 1 turns ratio	Eq 028	N_{PS1}		6.22
Result	Post calculated reflected voltage	Eq 030	V_{RPost}	[V]	77.16
Result	Post calculated maximum duty cycle	Eq 031	$D_{MaxPost}$		0.43
Result	Duty cycle prime	Eq 032	D_{Max}'		0.56
Result	Actual flux density	Eq 033	B_{MaxAct}	[T]	0.281
Result	Maximum DC input voltage for CCM operation	Eq 034	$V_{DCmaxCCM}$	[V]	267.23

Transformer winding design

Input	Margin according to safety standard		M	[mm]	0
Input	Copper space factor		f_{Cu}		0.4
Result	Effective bobbin window	Eq 035	BW_E	[mm]	11.0
Result	Effective winding cross-section	Eq 036	A_{Ne}	[mm²]	34.0
Input	Primary winding area factor		AF_{NP}		0.50
Input	Secondary 1 winding area factor		AF_{NS1}		0.45
Input	Auxiliary winding area factor		AF_{NVcc}		0.05

Primary winding

Result	Calculated wire copper cross-sectional area	Eq 037	A_{PCal}	[mm²]	0.1214
Result	Calculated maximum wire size	Eq 038	AWG_{PCal}		26
Input	Select wire size		AWG_P		28
Input	Select number of parallel wire		nw_P		1
Result	Wire copper diameter	Eq 039	d_P	[mm]	0.32
Result	Wire copper cross-sectional area	Eq 040	A_P	[mm²]	0.0821
Result	Wire current density	Eq 041	S_P	[A/mm²]	3.94
Input	Insulation thickness		INS_P	[mm]	0.01
Result	Turns per layer	Eq 042	NL_P	Turns/layer	32
Result	Number of layers	Eq 043	Ln_P	Layers	2

Secondary 1 winding

Result	Calculated wire copper cross-sectional area	Eq 044	A_{NS1Cal}	[mm²]	0.6800
Result	Calculated maximum wire size	Eq 045	AWG_{S1Cal}		19
Input	Select wire size		AWG_{S1}		31
Input	Select number of parallel wire		nw_{S1}		7
Result	Wire copper diameter	Eq 046	d_{S1}	[mm]	0.2881

Result	Wire copper cross-sectional area	Eq 047	A_{S1}	[mm²]	0.4562
Result	Peak current	Eq 048	I_{S1Max}	[A]	4.4677
Result	RMS current	Eq 049	I_{S1RMS}	[A]	2.2952
Result	Wire current density	Eq 050	S_{S1}	[A/mm²]	5.03
Input	Insulation thickness		INS_{S1}	[mm]	0.04
Result	Turns per layer	Eq 051	NL_{S1}	Turns/layer	4
Result	Number of layers	Eq 052	Ln_{S1}	Layers	3

RCD clamper and CS resistor

RCD clamper circuit

Input	Leakage inductance percentage		$L_{LK\%}$	[%]	1
Result	Leakage inductance	Eq 062	L_{LK}	[H]	7.01E-06
Result	Clamping voltage	Eq 063	V_{Clamp}	[V]	248.08
Result	Calculated clamping capacitor	Eq 064	$C_{ClampCal}$	[nF]	0.04
Input	Select clamping capacitor value (C2)		C_{clamp}	[nF]	0.22
Result	Calculated clamping resistor	Eq 065	$R_{clampCal}$	[kΩ]	442.0
Input	Select clamping resistor value (R4)		R_{clamp}	[kΩ]	200

CS resistor

Input	CS threshold value from datasheet		V_{CS_N}	[V]	0.8
Result	Calculated CS resistor (R8A, R8B)	Eq 066	R_{sense}	[Ω]	1.11

Output rectifier

Secondary 1 output rectifier

Result	Diode reverse voltage	Eq 067	$V_{RDiode1}$	[V]	72.23
Result	Diode RMS current		I_{S1RMS}	[A]	2.30
Input	Max. voltage undershoot at output capacitor		ΔV_{Out1}	[V]	0.24
Input	Number of clock periods		n_{cp1}		20
Result	Output capacitor ripple current	Eq 068	$I_{Ripple1}$	[A]	1.74
Result	Calculated minimum output capacitor	Eq 069	$C_{Out1Cal}$	[µF]	1000
Input	Select output capacitor value (C152)		C_{Out1}	[µF]	1000
Input	ESR (Z_{max}) value from datasheet at 100 kHz		R_{ESR1}	[Ω]	0.028
Input	Number of parallel capacitors		nc_{COut1}		1
Result	Zero frequency of output capacitor	Eq 070	f_{ZCOut1}	[kHz]	5.68
Result	First-stage ripple voltage	Eq 071	$V_{Ripple1}$	[V]	0.125094
Input	Select LC filter inductor value (L151)		L_{out1}	[µH]	2.2
Result	Calculated LC filter capacitor	Eq 072	C_{LCCal1}	[µF]	356.4
Input	Select LC filter capacitor value (C153)		C_{LC1}	[µF]	470
Result	LC filter frequency	Eq 073	f_{LC1}	[kHz]	4.95
Result	Second-stage ripple voltage	Eq 074	$V_{2ndRipple1}$	[mV]	0.20

V_{CC} diode and capacitor

V_{CC} diode and capacitor

Result	Auxiliary diode reverse voltage (D2)	Eq 083	$V_{RDiodeVCC}$	[V]	80.10
Input	Soft-start time from datasheet		t_{ss}	[ms]	12
Input	$I_{VCC,Charge3}$ from datasheet		$I_{VCC\_Charge3}$	[mA]	3
Input	V_{CC} on-threshold		V_{VCC_ON}	[V]	16
Input	V_{CC} off-threshold		V_{VCC_OFF}	[V]	10
Result	Calculated V_{CC} capacitor	Eq 084	C_{VCCCal}	[µF]	6.00
Input	Select V_{CC} capacitor (C3)		C_{VCC}	[µF]	22
Input	V_{CC} short threshold from datasheet		V_{VCC_SCP}	[V]	1.1
Input	$I_{VCC\_Charge1}$ from datasheet		$I_{VCC\_Charge1}$	[mA]	0.2
Result	Start-up time	Eq 085	$t_{StartUp}$	[ms]	230.267

Appendix A: Transformer design and spreadsheet [4]

Calculation of losses

Input diode bridge

Input	Diode bridge forward voltage		V_{FBR}	[V]	1
Result	Diode bridge power loss	Eq 086	P_{DIN}	[W]	0.91

Transformer copper

Result	Primary winding copper resistance	Eq 087	R_{PCu}	[mΩ]	483.34
Result	Secondary 1 winding copper resistance	Eq 088	R_{S1Cu}	[mΩ]	13.98
Result	Primary winding copper loss	Eq 090	P_{PCu}	[mW]	50.52
Result	Secondary 1 winding copper loss	Eq 091	P_{S1Cu}	[mW]	73.64
Result	Total transformer copper loss	Eq 093	P_{Cu}	[W]	0.1242

Output rectifier diode

Result	Secondary 1 diode loss	Eq 094	P_{Diode1}	[W]	0.92

RCD clamper circuit

Result	RCD clamper loss	Eq 096	$P_{Clamper}$	[W]	0.30

CS resistor

Result	CS resistor loss	Eq 097	P_{CS}	[W]	0.12

MOSFET

Input	R_{DSON} from datasheet		R_{DSON} at T_J=125°C	[Ω]	2.28
Input	Co(er) from datasheet		$C_{o(er)}$	[pF]	10
Input	External drain-to-source capacitance		C_{DS}	[pF]	0
Result	Switch-on loss at minimum AC input voltage	Eq 098	$P_{SONMinAC}$	[W]	0.0197
Result	Conduction loss at minimum AC input voltage	Eq 099	$P_{condMinAC}$	[W]	0.2383
Result	Total MOSFET loss at minimum AC input voltage	Eq 100	$P_{MOSMinAC}$	[W]	0.2580
Result	Switch-on loss at maximum AC input voltage	Eq 101	$P_{SONMaxAC}$	[W]	0.1276
Result	Conduction loss at maximum AC input voltage	Eq 102	$P_{condMaxAC}$	[W]	0.0658
Result	Total MOSFET loss at maximum AC input voltage	Eq 103	$P_{MOSMaxAC}$	[W]	0.1934
Result	Total MOSFET loss (from minimum or maximum AC)		P_{MOS}	[W]	0.2580

Controller

Input	Controller current consumption		I_{VCC_Normal}	[mA]	0.9
Result	Controller loss	Eq 104	P_{Ctrl}	[W]	0.0119

Efficiency after losses

Result	Total power loss	Eq 105	P_{Losses}	[W]	2.63
Result	Post calculated efficiency	Eq 106	η_{Post}	%	87.24%

CoolSET™/MOSFET temperature

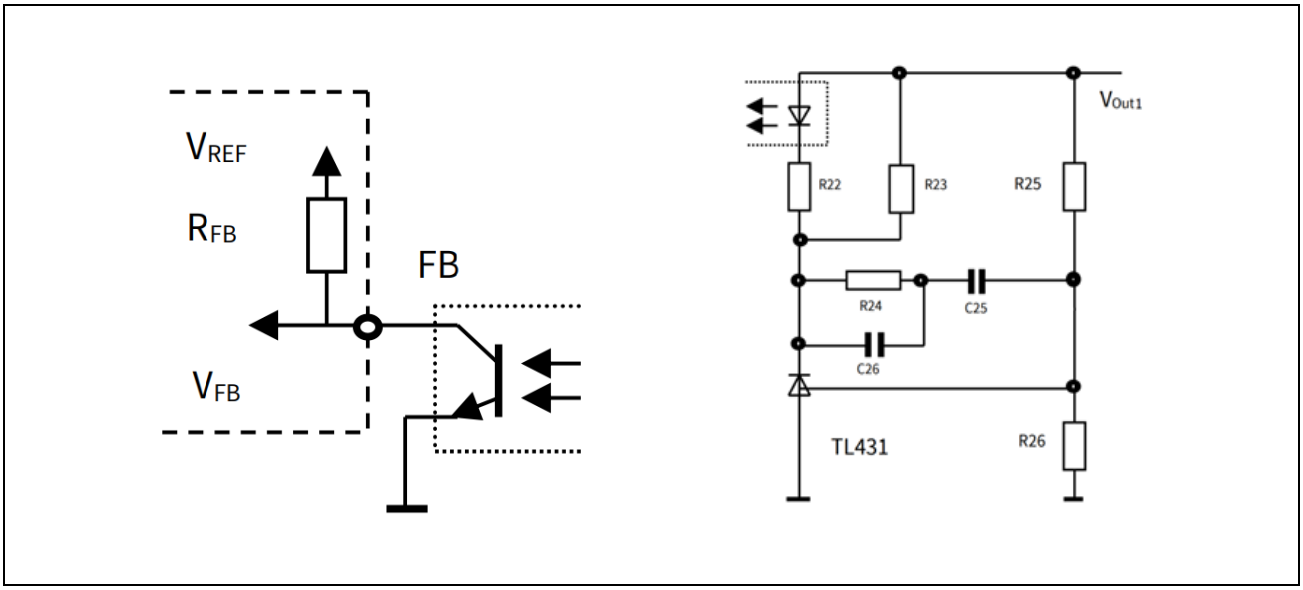
CoolSET™/MOSFET temperature

Input	Enter thermal resistance junction-ambient (include copper pour)		R_{thJA_As}	[°K/W]	160.0
Result	Temperature rise	Eq 107	ΔT	[°K]	41.3
Result	Junction temperature at T_{amax}	Eq 108	Tjmax	°C	81.3

Appendix A: Transformer design and spreadsheet [4]

Output regulation (isolated using TL431 and optocoupler)

Isolated feedback circuit



Output regulation

Input	TL431 reference voltage		V_{REF_TL}	[V]	2.5
Input	Current for voltage divider resistor R26		I_{R26}	[mA]	0.2
Result	Calculated voltage divider resistor	Eq 111	$R26_{Cal}$	[kΩ]	12.5
Input	Select voltage divider resistor value		R26	[kΩ]	12
Result	Calculated voltage divider resistor	Eq 112	$R25_{Cal}$	[kΩ]	45.60
Input	Select voltage divider resistor value		R25	[kΩ]	47.0

Optocoupler and TL431 bias

Input	Current transfer ratio (CTR)		G_C	[%]	200%
Input	Optocoupler diode forward voltage		V_{FOpto}	[V]	1.25
Input	Maximum current for optocoupler diode		I_{Fmax}	[mA]	50
Input	Minimum current for TL431		I_{KAmin}	[mA]	1
Result	Calculated minimum optocoupler bias resistance	Eq 114	$R22_{Cal}$	[kΩ]	0.1650
Input	Select optocoupler bias resistor		R22	[kΩ]	0.82
Input	FB pull-up reference voltage V_{REF} from datasheet		V_{REF}	[V]	3.3
Input	V_{FB_OLP} from datasheet		V_{FB_OLP}	[V]	2.75
Input	R_{FB} from datasheet		R_{FB}	[kΩ]	15
Result	Calculated maximum TL431 bias resistance	Eq 115	$R23_{Cal}$	[kΩ]	1.27
Input	Selected TL431 bias resistor		R23	[kΩ]	1.2

Regulation loop

Result	FB transfer characteristic	Eq 116	K_{FB}		36.59
Result	Gain of FB transfer characteristic	Eq 117	G_{FB}	[dB]	31.27
Result	Voltage divider transfer characteristic	Eq 118	K_{VD}		0.208333
Result	Gain of voltage divider transfer characteristic	Eq 119	G_{VD}	[dB]	-13.62
Result	Resistance at maximum load pole	Eq 120	R_{LH}	[Ω]	8.00
Result	Resistance at minimum load pole	Eq 121	R_{LL}	[Ω]	72.00
Result	Poles of power stage at maximum load pole	Eq 122	f_{OH}	[Hz]	39.79
Result	Poles of power stage at minimum load pole	Eq 123	f_{OL}	[Hz]	4.42
Result	Zero frequency of the compensation network	Eq 124	f_{OM}	[Hz]	13.26
Input	Zero dB crossover frequency		fg	[kHz]	2
Input	PWM-OP gain from datasheet		A_V		2.03
Result	Transient impedance	Eq 117	Z_{PWM}	[V/A]	2.8
Result	Power stage at crossover frequency	Eq 118	$\|F_{PWR}(fg)\|$		0.124

Result	Gain of power stage at crossover frequency	Eq 119	$G_{PWR}(fg)$	[db]	-18.16
Result	Gain of the regulation loop at fg	Eq 120	Gs(ω)	[db]	-0.522
Result	Separated components of the regulator	Eq 121	Gr(ω)	[db]	0.522
Result	Calculated resistance value of compensation network	Eq 122	$R24_{Cal}$	[kΩ]	10.15
Input	Select resistor value of compensation network		R24	[kΩ]	10
Result	Calculated capacitance value of compensation network	Eq 123	$C26_{Cal}$	[nF]	7.958
Input	Select capacitor value of compensation network		C26	[nF]	1
Result	Calculated capacitance value of compensation network	Eq 124	$C25_{Cal}$	[nF]	1199.00
Input	Select capacitor value of compensation network		C25	[nF]	100

Final design

Electrical

Minimum AC voltage			[V]	90
Maximum AC voltage			[V]	265
Maximum input current			[A]	0.23
Minimum DC voltage			[V]	100
Maximum DC voltage			[V]	375
Maximum output power			[W]	18.0
Output voltage 1			[V]	12.0
Output ripple voltage 1			[mV]	0.2
Transformer peak current			[A]	0.72
Maximum duty cycle				0.43
Reflected voltage			[V]	77
Copper losses			[W]	0.12
MOSFET losses			[W]	0.26
Sum losses			[W]	2.63
Efficiency			[%]	87.24%

Transformer

Core type				EE20/10/6
Core material				TP4A(TDG)
Effective core area			[mm^2]	32
Maximum flux density			[mT]	281
Inductance			[µH]	701
Margin			[mm]	0
Primary turns			turns	56
Primary copper wire size			AWG	28
Number of primary copper wire in parallel				1
Primary layers			Layer	2
Secondary 1 turns (N_{S1})			Turns	9
Secondary 1 copper wire size			AWG	29
Number of secondary 1 copper wire in parallel				7
Secondary 1 layers			Layer	3
Auxiliary turns			Turns	10
Leakage inductance			[µH]	7.0

Components

Input capacitor (C1)			[µF]	44.0
Secondary 1 output capacitor (C152)			[µF]	1000.0
Secondary 1 output capacitor in parallel				1.0
Secondary 1 LC filter inductor (L151)			[µH]	2.2
Secondary 1 LC filter capacitor (C153)			[µF]	470.0
V_{CC} capacitor (C3)			[µF]	22.0
Sense resistor (R8A, R8B)			[Ω]	1.11
Clamping resistor (R4)			[kΩ]	200.0
Clamping capacitor (C2)			[nF]	0.22

Regulation components (isolated using TL431 and optocoupler)

Appendix A: Transformer design and spreadsheet [4]

Voltage divider		R26	[kΩ]	12.0
Voltage divider (V_{out1} sense)		R25	[kΩ]	47.0
Optocoupler bias resistor		R22	[kΩ]	0.82
TL431 bias resistor		R23	[kΩ]	1.2
Compensation network resistor		R24	[kΩ]	10.0
Compensation network capacitor		C26	[nF]	1.00
Compensation network capacitor		C25	[nF]	100.0

12 Appendix B: WE transformer specification

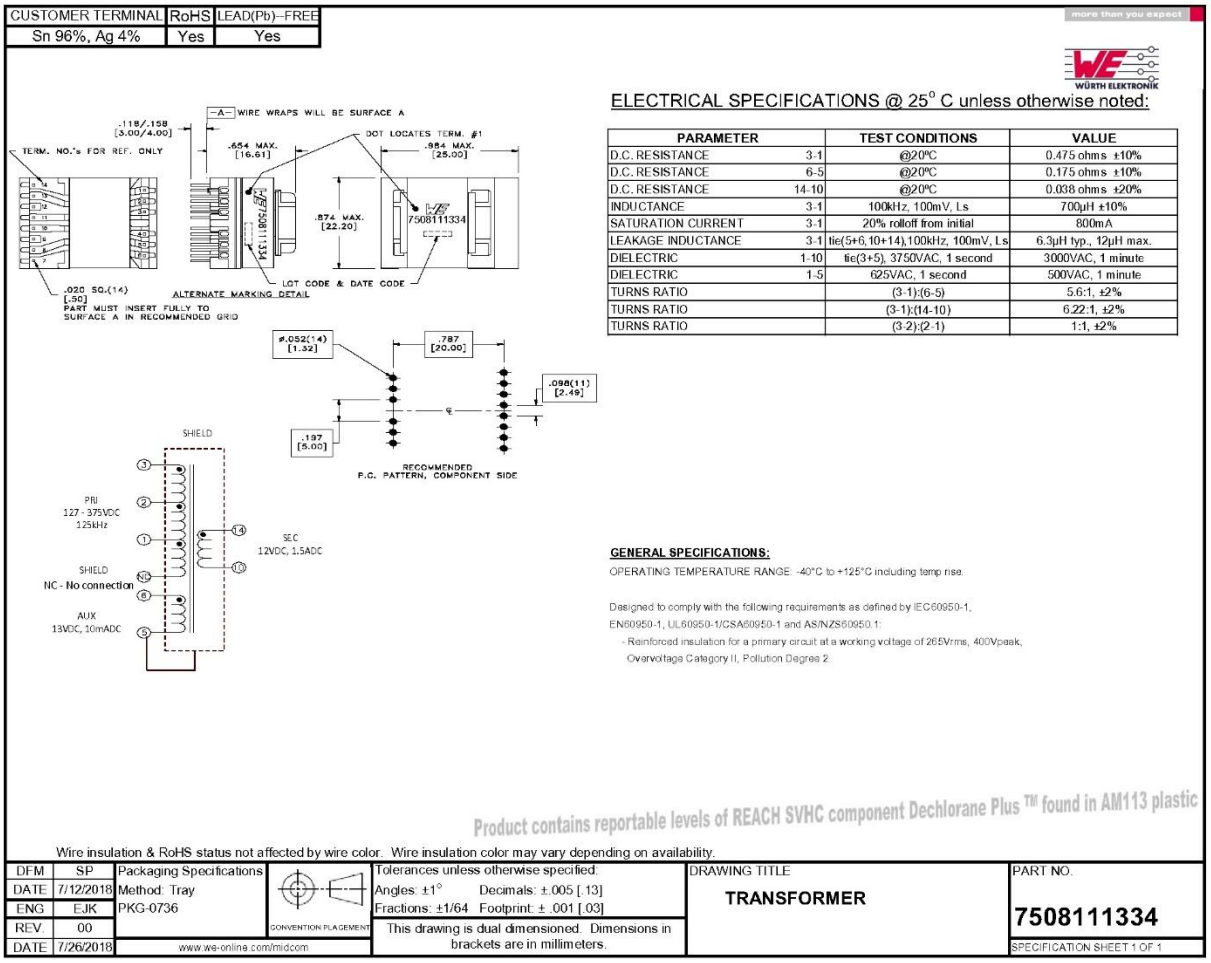


Figure 37 Transformer structure

13 References

[1] ICE5xSAG datasheet

[2] IPN70R1K2P7S datasheet

[3] Design guide 5th generation fixed-frequency design guide – ICE5xSAG and ICE5xRxxxxAG

[4] Calculation tool – ICE5xSAG and ICE5xRxxxxAG

Revision history

Document version	Date of release	Description of changes
V 1.0	6 August 2018	First release

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