Fifth-Generation Fixed-Frequency Design Guide

Design Guide - ICE5xSAG and ICE5xRxxxxAG

About this document

Scope and purpose

This document is a design guide for a fixed-frequency Flyback converter using Infineon's newest fifth-generation fixed-frequency PWM controller, ICE5xSAG, and CoolSET™, ICE5xRxxxxAG, which offer high-efficiency, low-standby power with selectable entry and exit standby power options, wider V_{CC} operating range with fast start-up, robust line protection with input Line Over Voltage Protection (LOVP), and various protection modes for a highly reliable system.

Intended audience

This document is intended for power-supply design/application engineers, students, etc. who wish to design power supplies with Infineon's newest fifth-generation fixed-frequency PWM controller, ICE5xSAG, and CoolSET™, ICE5xRxxxxAG.

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1 Abstract

This design guide for a fixed-frequency Flyback converter using Infineon's newest fifth-generation fixed-frequency PWM controller, ICE5xSAG, and CoolSET™, ICE5xRxxxxAG.

The IC is optimized for off-line SMPS applications including home appliances/white goods, TVs, PCs, servers, Blu-ray players, set-top boxes and notebook adapters. The frequency reduction with soft gate-driving and frequency-jitter operation offers lower EMI and better efficiency between light and medium loads. The selectable entry/exit standby power Active Burst Mode (ABM) enables flexibility and low power consumption in standby mode with small and controllable output voltage ripple. The product has a wide operating range (10~25.5 V) of IC power supply and lower power consumption. The numerous protection functions with input LOVP give full protection to the power supply system in failure situations. All of these features make the ICE5xSAG/ICE5xRxxxxAG an outstanding PWM controller/CoolSET™ for fixed-frequency Flyback converters.

2 Description

2.1 List of features

- Integrated 700 V/ 800 V avalanche rugged CoolMOS™
- Enhanced ABM with selectable entry and exit standby power
- Digital frequency reduction for better overall system efficiency
- Fast start-up, achieved with cascode configuration
- Discontinuous Conduction Mode (DCM) and Continuous Conduction Mode (CCM) operation with slope compensation
- Frequency jitter and soft gate-driving for low EMI
- Built-in digital soft-start
- Cycle-to-cycle Peak Current Limitation (PCL)
- Integrated error amplifier to support direct feedback (FB) in a non-isolated Flyback converter
- Comprehensive protection with input LOVP, V_{CC} OV, V_{CC} Under Voltage (UV), over-load/open-loop, over-temperature and Current Sense (CS) short-to-GND
- All protections are in auto-restart mode
- Limited charging current for V_{CC} short-to-GND
- Pb-free lead plating, halogen-free mold compound, RoHS compliant

2.2 Pin configuration and functionality

The pin configuration is shown in Figure 1 and the functions are described inTable 1.

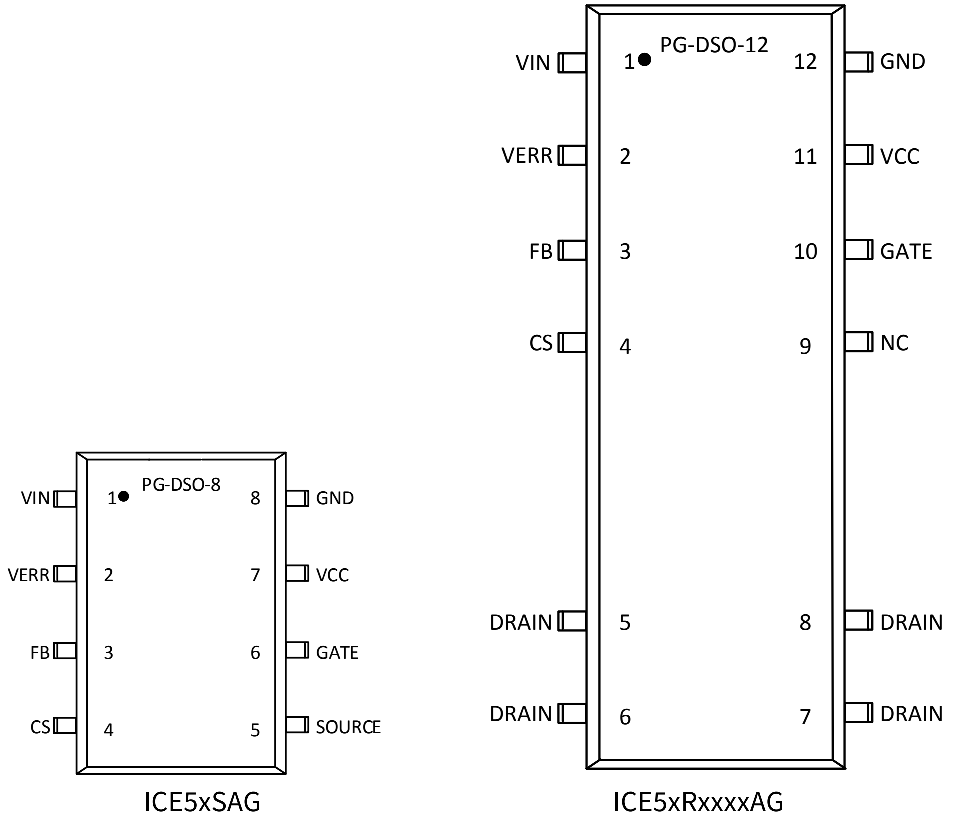

Figure 1 Pin configuration

Table 1 Pin definitions and functions

Pin		Symbol	Function
ICE5xSAG	ICE5xRxxxxAG		
1	1	VIN	Input LOVP The VIN pin is connected to the bus via a resistor divider (see Figure 2) to sense the line voltage. Internally, it is connected to the LOV comparator, which will stop the switching when a LOVP condition occurs. To disable LOVP, connect this pin to GND.
2	2	VERR	Error amplifier The VERR pin is internally connected to the transconductance error amplifier for non-isolated Flyback applications. Connect this pin to GND for isolated Flyback applications.
3	3	FB	FB and ABM entry/exit control The FB pin combines the functions of FB control, selectable burst entry/exit control and over-load/open-loop protection.
4	4	CS	CS The CS pin is connected to the shunt resistor for the primary current sensing externally and to the PWM signal generator block for switch-off determination (together with the FB voltage) internally. CS short-to-GND protection is also sensed via this pin.
5	-	SOURCE	Source The SOURCE pin is connected to the source of the external power MOSFET (see Figure 2), which is in series with the internal low-side MOSFET and internal V_{CC} diode D.
-	5, 6, 7, 8	DRAIN	Drain (drain of integrated CoolMOS™) The DRAIN pin is connected to the drain of the integrated CoolMOS™.
-	9	NC	No connection
6	10	GATE	Gate driver output The GATE pin is connected to the gate of the power MOSFET, and a pull-up resistor is connected from the bus voltage to turn on the power MOSFET for charging up the V_{CC} capacitor during start-up.
7	11	V_{CC}	V_{CC} (positive voltage supply) The V_{CC} pin is the positive voltage supply to the IC. The operating range is between V_{VCC_OFF} and V_{VCC_OVP}.
8	12	GND	Ground The GND pin is the common ground of the controller.

3 Overview of fixed-frequency Flyback converter

Figure 2 and Figure 3 show the typical application of ICE5xSAG and ICE5xRxxxxAG in an isolated fixed-frequency Flyback converter using TL431 and an optocoupler.

Figure 4 and Figure 5 show the typical application of ICE5xSAG and ICE5xRxxxxAG in a non-isolated fixed-frequency Flyback converter using an integrated error amplifier.

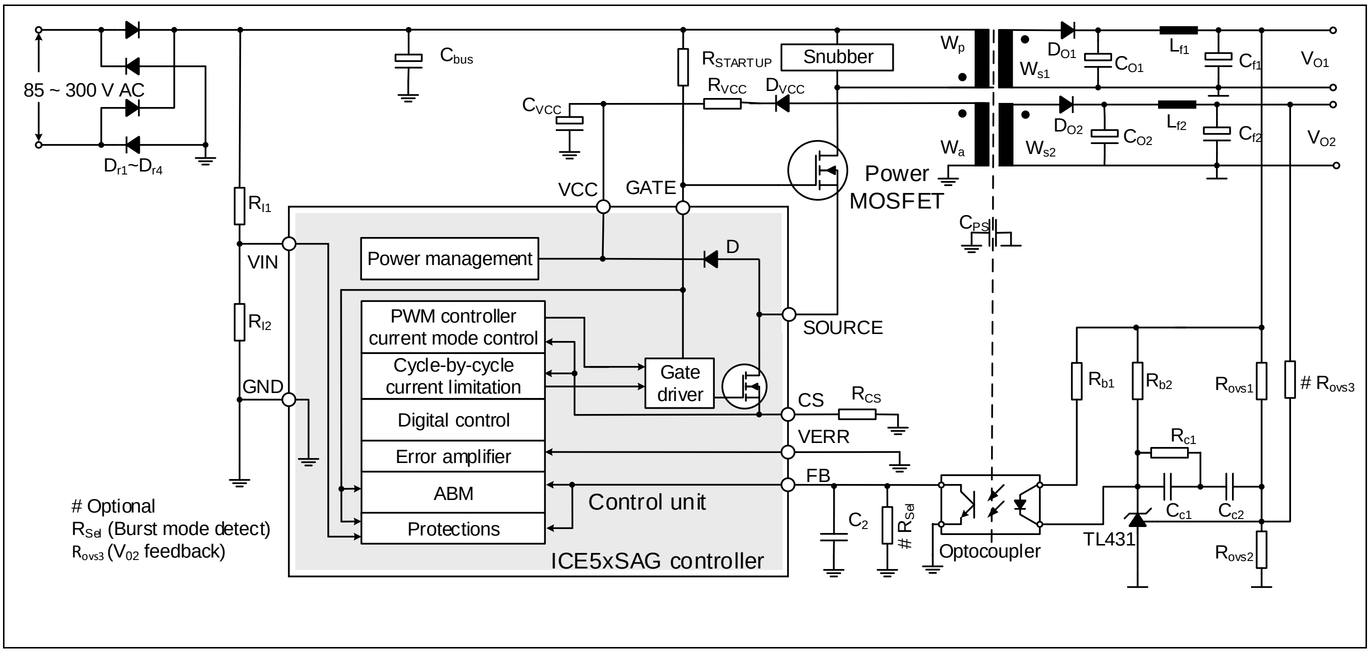

Figure 2 Typical application of the PWM controller in an isolated fixed-frequency Flyback converter using TL431 and an optocoupler

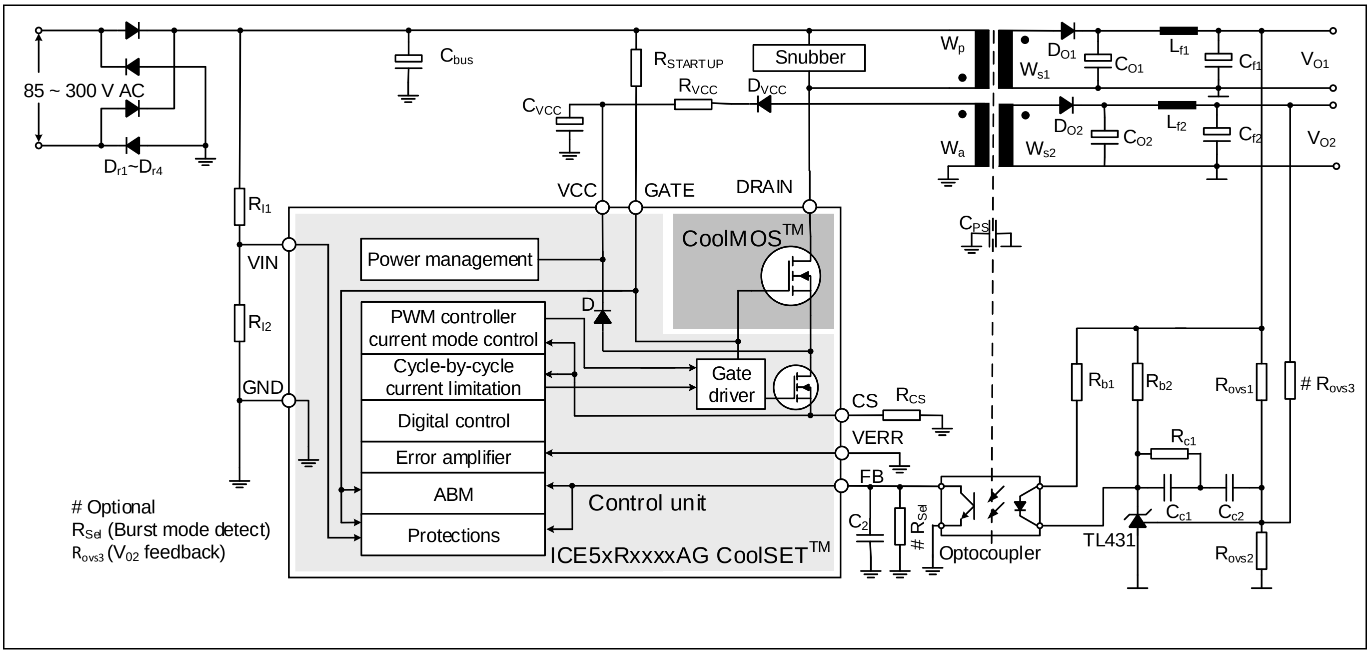

Figure 3 Typical application of the CoolSET™ in an isolated fixed-frequency Flyback converter using TL431 and an optocoupler

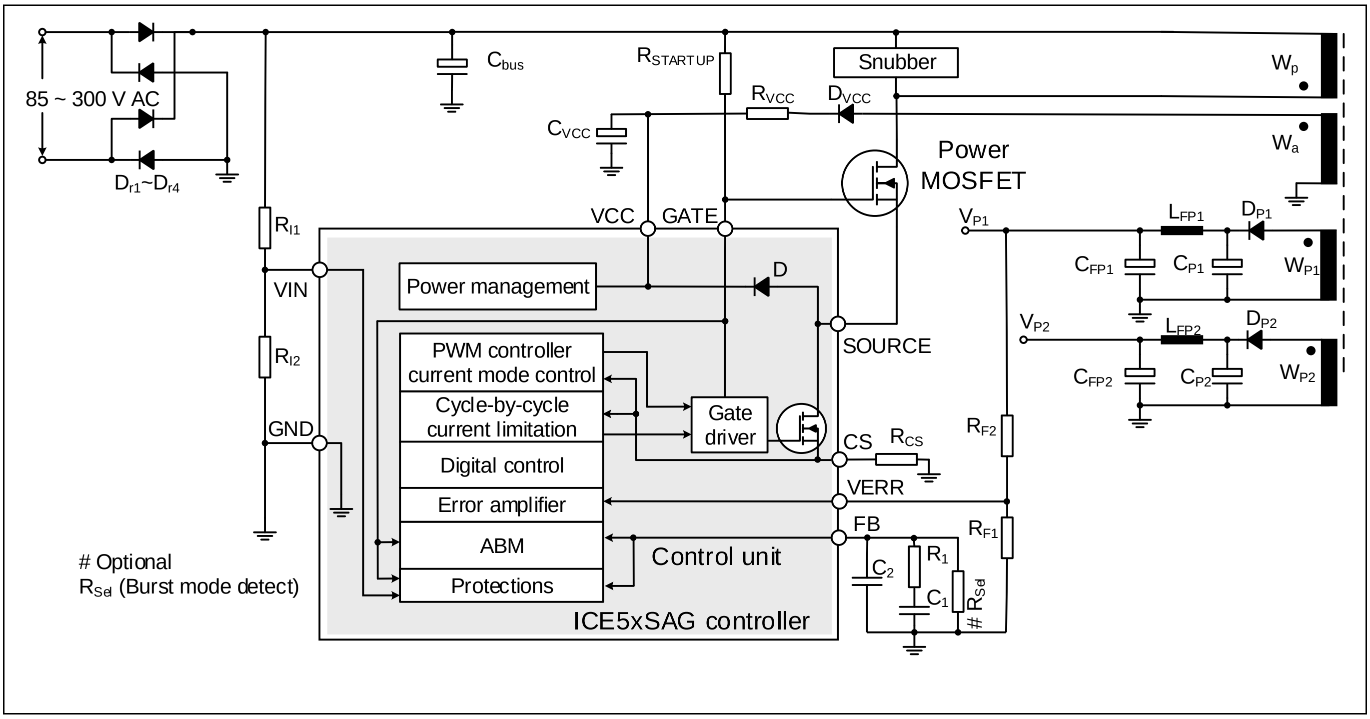

Figure 4 Typical application of the PWM controller in a non-isolated Flyback converter using an integrated error amplifier

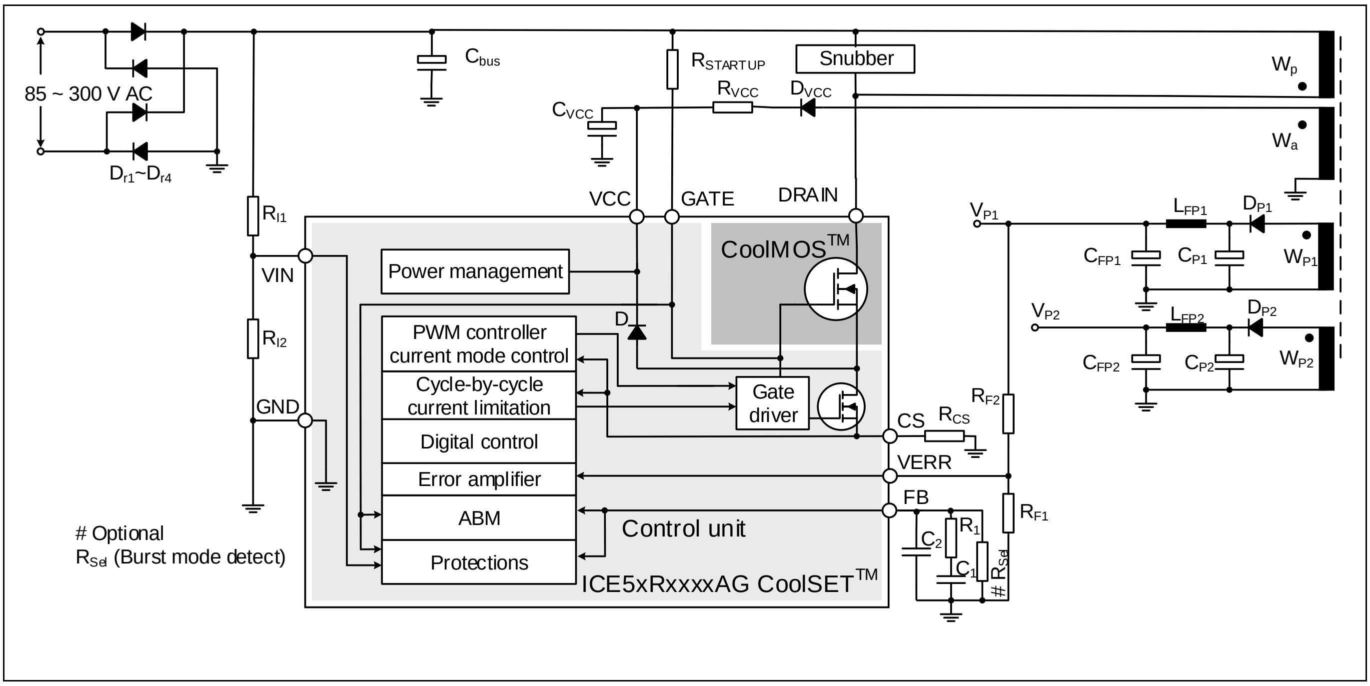

Figure 5 Typical application of the CoolSET™ in a non-isolated Flyback converter using an integrated error amplifier

4 Functional description and component design

4.1 V_{CC} pre-charging and typical V_{CC} voltage during start-up

When AC-line input voltage is applied, a rectified voltage appears across the capacitor C_{bus} (see Figure 2). The pull-up resistor $R_{StartUp}$ provides a current to charge the C_{iss} (input capacitance) of the power MOSFET, generating one voltage level. If the voltage across C_{iss} is sufficiently high, the power MOSFET will turn on and the V_{CC} capacitor will be charged through primary inductance of transformer L_P, the power MOSFET and the internal diode with two steps of constant current source $I_{VCC\_Charge1}$[1] and $I_{VCC\_Charge3}$[1].

A very small constant current source ($I_{VCC\_Charge1}$) charges the V_{CC} capacitor until V_{CC} reaches V_{VCC_SCP} to protect the controller from a V_{CC} pin short-to-GND during start-up. After this, the second step constant current source ($I_{VCC\_Charge3}$) is provided to further charge the V_{CC} capacitor, until V_{CC} exceeds the turn-on threshold V_{VCC_ON}. As shown in Phase I in Figure 6, the V_{CC} voltage increases almost linearly, with two steps.

Note: The recommended typical value for $R_{StartUp}$ is 50 MΩ (20 MΩ~100 MΩ). $R_{StartUp}$ value is directly proportional to $t_{StartUp}$ and inversely proportional to no-load standby power.

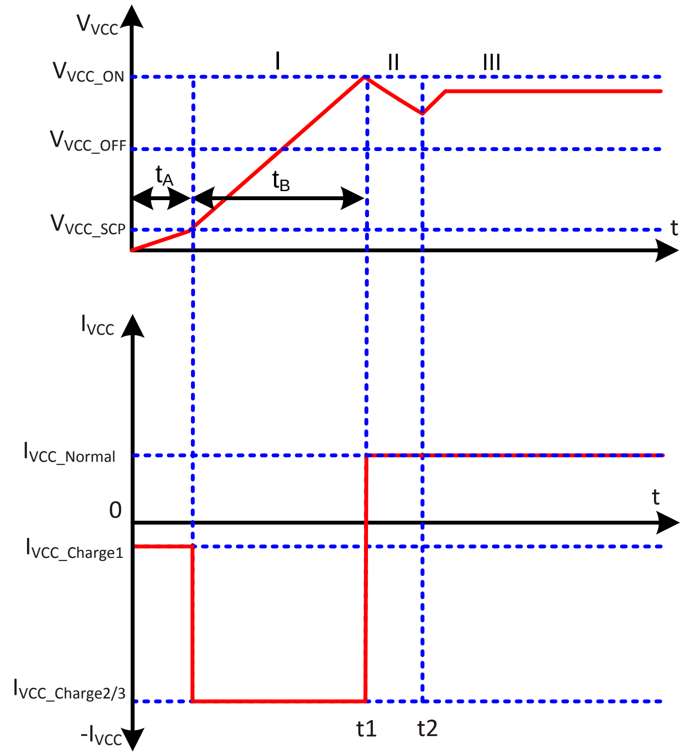

Figure 6 V_{CC} voltage and current at start-up

The time taken for the V_{CC} pre-charging can then be approximated as:

$$t_{\mathrm{StartUp}} = t_{\mathrm{A}} + t_{\mathrm{B}} = \frac{V_{VCC\_SCP} \cdot C_{VCC}}{I_{VCC\_Charge1}} + \frac{(V_{VCC\_ON} - V_{VCC\_SCP}) \cdot C_{VCC}}{I_{VCC\_Charge3}} \quad \text{(Eq 201)}$$

[1] $I_{VCC\_Charge1/2/3}$ is charging current from the controller to the V_{CC} capacitor during start-up

where V_{VCC_SCP} : V_{CC} short-circuit protection voltage

C_{VCC} : V_{CC} capacitor

V_{VCC_ON} : V_{CC} turn-on threshold voltage

$I_{VCC\_Charge1}$: V_{CC} charge current 1

$I_{VCC\_Charge3}$: V_{CC} charge current 3

When the V_{CC} voltage exceeds the V_{VCC_ON} at time t_1, the IC begins to operate with a soft-start. Due to power consumption of the IC and the fact that there is still no energy from the auxiliary winding to charge the V_{CC} capacitor before the output voltage is built up, the V_{CC} voltage drops (Phase II). Once the output voltage rises close to regulation, the auxiliary winding starts to charge the V_{CC} capacitor from the time t_2 onward, delivering the power to the IC. The V_{CC} will then reach a constant value depending on output load.

4.1.1 V_{CC} capacitor

Since there is a V_{CC} UV protection, the V_{CC} capacitor should be selected to be large enough to ensure that enough energy is stored in the V_{CC} capacitor so that the V_{CC} voltage will not drop below the V_{CC} UV protection threshold V_{VCC_OFF} before the auxiliary power kicks in. Therefore, the minimum capacitance should fulfill the following requirement:

$$C_{VCC} > \frac{I_{VCC\_Charge3} \times t_{ss}}{V_{VCC\_ON} - V_{VCC\_OFF}} \qquad \text{(Eq 202)}$$

where C_{VCC} : V_{CC} capacitor

$I_{VCC\_Charge3}$: V_{CC} charge current 3

t_{ss} : soft-start time

During ABM condition where the auxiliary winding cannot provide enough power to supply the IC because of the burst switching, the V_{CC} voltage may drop below the V_{VCC_OFF}. Therefore the capacitance needs to be increased, as the calculation above may not be enough.

4.2 Soft-start

After the supply voltage of the IC exceeds 16 V, which corresponds to t_1 of Figure 6, the IC starts switching with a soft-start. The soft-start implemented is a digital time-based function. The preset soft-start time is t_{SS} (12 ms) with four steps (see Figure 7). If not limited by other functions, the peak voltage on the CS pin will increase incrementally from 0.3 V to V_{CS_N} (0.8 V). The normal FB loop will take over the control when the output voltage reaches its regulated value.

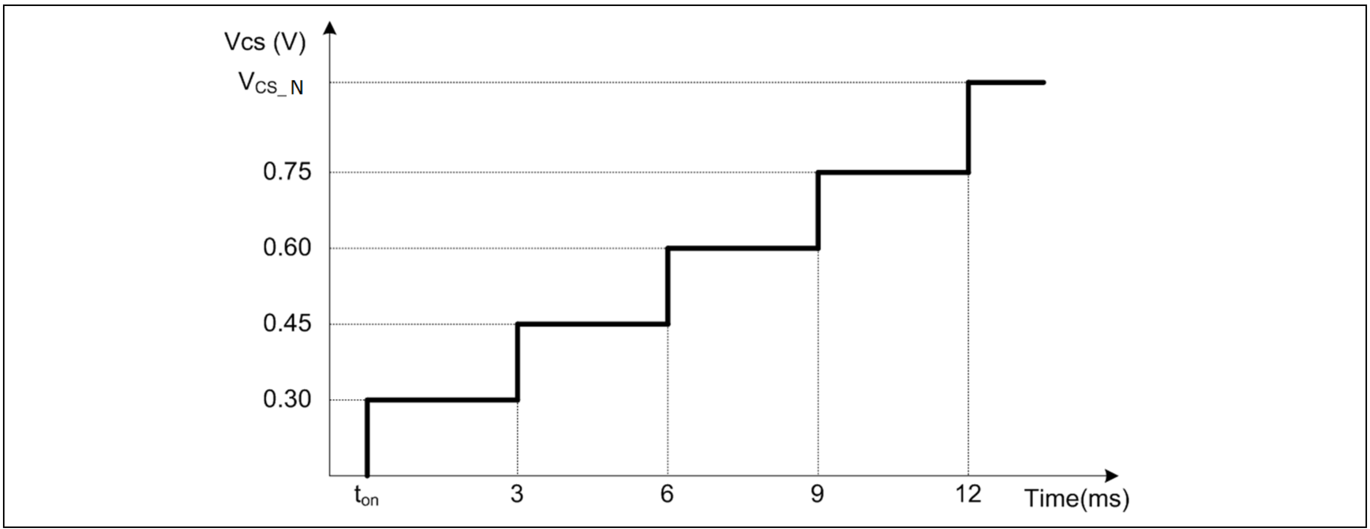

Figure 7 Maximum CS voltage during soft-start

4.3 Normal operation

During normal operation the PWM controller consists of a digital signal processing circuit, including regulation control, and an analog circuit, including a current measurement unit and a comparator. Details of normal operation are illustrated in the following paragraphs.

4.3.1 PWM operation and peak current mode control

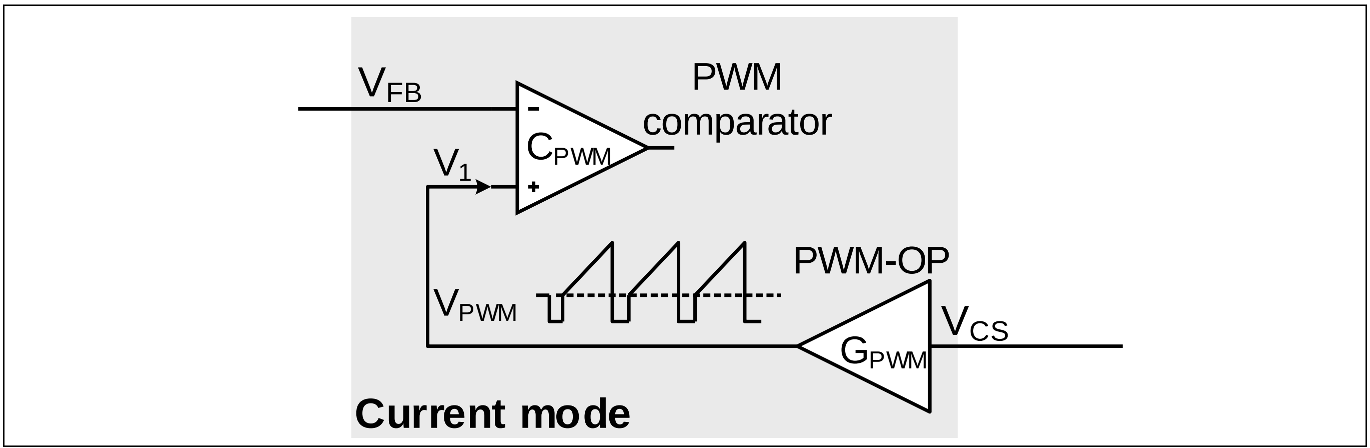

Figure 8 PWM block

4.3.1.1 Switch-on determination

The power MOSFET turn-on is synchronized with the internal oscillator, with a switching frequency f_{SW} that corresponds to the voltage level V_{FB} (see Figure 10).

4.3.1.2 Switch-off determination

In peak current mode control, the PWM comparator monitors voltage V_1 (see Figure 8), which is the representation of the instantaneous current of the power MOSFET. When V_1 exceeds V_{FB}, the PWM comparator sends a signal to switch off the gate of the power MOSFET. Therefore, the peak current of the power MOSFET is controlled by the FB voltage V_{FB} (see **Error! Reference source not found.**).

At switch-on transient of the power MOSFET, a voltage spike across R_{CS} can cause V_1 to increase and exceed V_{FB}. To avoid a false switch-off, the IC has a blanking time t_{CS_LEB} before detecting the voltage across R_{CS} to mask the voltage spike. Therefore, the minimum turn-on time of the power MOSFET is t_{CS_LEB}.

If the voltage level at V_1 takes a long time to exceed V_{FB}, the IC will implement a maximum duty cycle control to force the power MOSFET to switch off when D_{MAX} = 0.75.

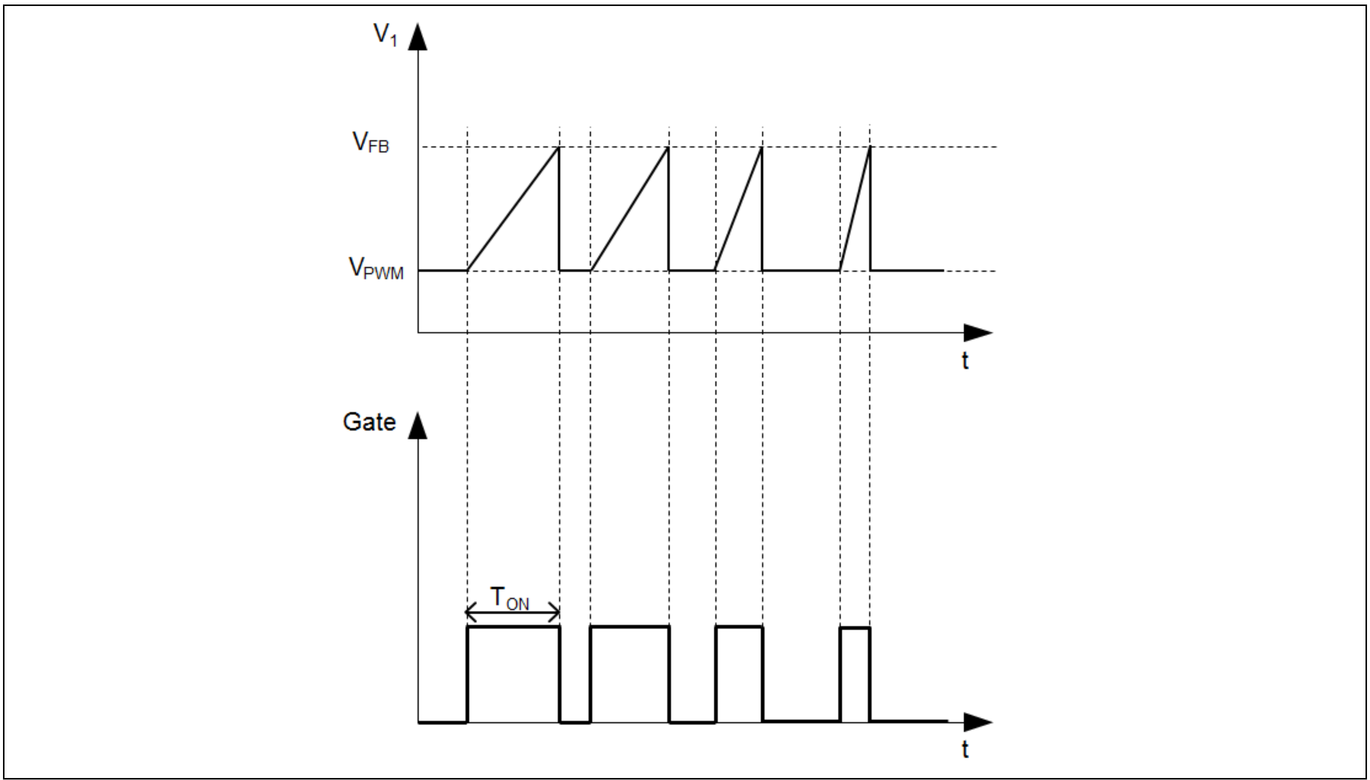

Figure 9 PWM

4.3.2 Current sensing

The power MOSFET current generates a voltage V_{CS} across the CS resistor R_{CS} connected between the CS pin and the GND pin. V_{CS} is amplified with gain G_{PWM}, then added with an offset V_{PWM} to become V_1, as described below.

$$V_{\mathrm{CS}} = I_{\mathrm{D}} \times R_{\mathrm{CS}} \tag{Eq 203}$$

$$V_1 = V_{\mathrm{CS}} * G_{\mathrm{PWM}} + V_{\mathrm{PWM}} \tag{Eq 204}$$

where V_{CS} : CS pin voltage

I_D : power MOSFET current

R_{CS} : resistance of the CS resistor

V_1 : voltage level compared to V_{FB} as described in section 4.3.1.2

G_{PWM} : PWM-OP gain

V_{PWM} : offset for voltage ramp

4.3.3 Frequency reduction

Frequency reduction is implemented to achieve better efficiency at light load. At light load, the reduced switching frequency f_{SW} improves efficiency by reducing the switching losses.

When load decreases, V_{FB} decreases as well. f_{SW} is dependent on the V_{FB} as shown in Figure 10. Therefore, f_{SW} decreases as the load decreases.

Typically, f_{SW} at high load is 100 kHz/125 kHz and starts to decrease at V_{FB} = 1.7 V. There is no further frequency reduction once it reaches the f_{OSCx_MIN} even the load is further reduced.

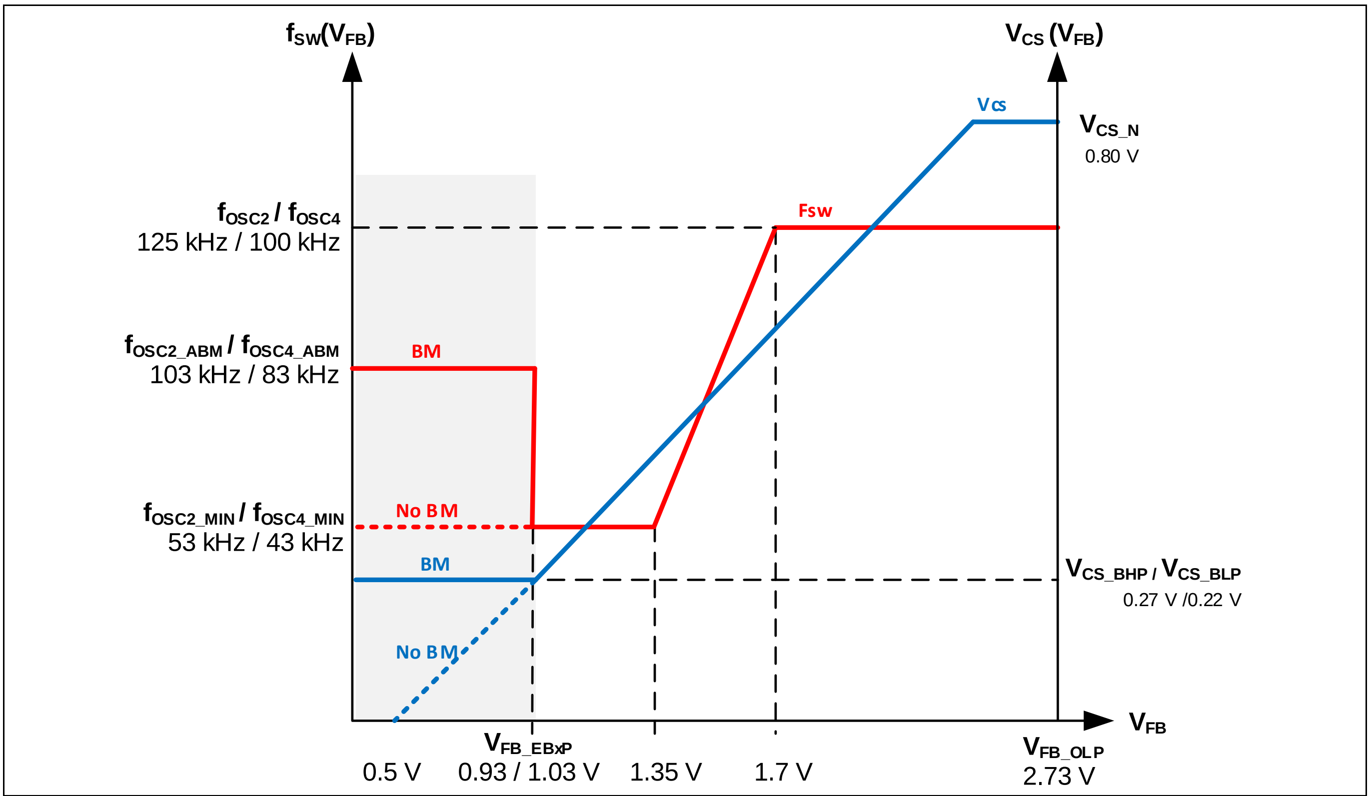

Figure 10 Frequency reduction curve

4.3.4 Slope compensation

In CCM operation, a duty cycle greater than 50 percent may generate a sub-harmonic oscillation. A small perturbation on the transformer flux φ can result in loop instability where the system cannot auto-correct itself, as can be seen in the figure below right, where $\Delta\varphi_2$ is greater than $\Delta\varphi_1$. $\Delta\varphi_2$ should be less than $\Delta\varphi_1$ for a system to be stable (figure below left). DCM operation is more stable, as the transformer flux always goes to zero.

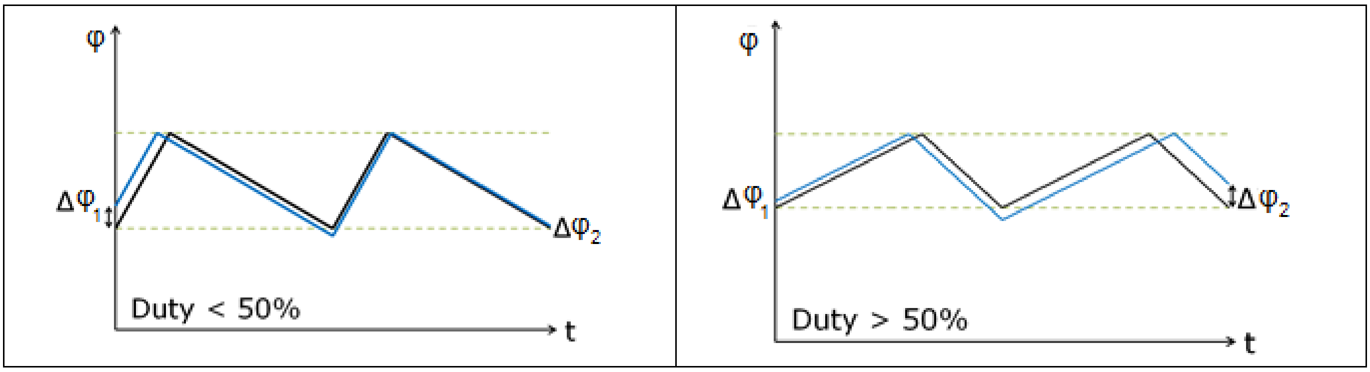

Figure 11 Perturbed transformer charging and discharging flux (black line stabilized transformer flux)

ICE5xSAG/ICE5xRxxxxAG can operate in CCM. To avoid the sub-harmonic oscillation, slope compensation is added to V_{CS} when the gate of the power MOSFET is turned on for more than 40 percent of the switching cycle period. The relationship between V_{FB} and the V_{CS} for CCM operation is described in the equation below:

$$V_{FB} = V_{CS} * G_{PWM} + V_{PWM} + M_{COMP} * (T_{ON} - 40\% * T_{PERIOD}) \quad \text{(Eq 205)}$$

where T_{ON} : gate turn-on time of the power MOSFET

M_{COMP} : slope compensation rate

T_{PERIOD} : switching cycle period

As a result of slope compensation, $\Delta\varphi_2$ is reduced to smaller than $\Delta\varphi_1$, and therefore the system is able to stabilize itself as shown in the figure below.

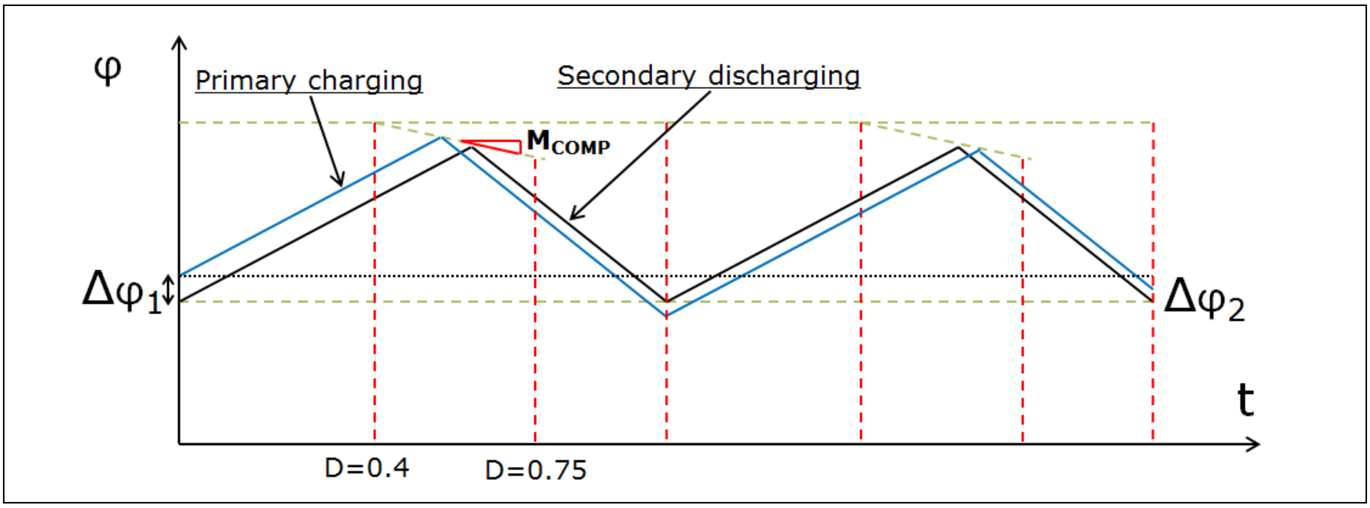

Figure 12 Perturbed transformer current with slope compensation

The slope compensation circuit is disabled and no slope compensation is added to the V_{CS} pin during ABM to save on power consumption.

4.3.5 Oscillator and frequency jittering

The oscillator generates a frequency of 100 kHz/125 kHz with frequency jittering of ±4 percent at a jittering period of T_{JITTER} (4 ms). The frequency jittering helps to reduce conducted EMI.

A capacitor, current source and current sink which determine the frequency are integrated. The charging and discharging current of the implemented oscillator capacitor are internally trimmed in order to achieve a highly accurate switching frequency.

Once the soft-start period is over and when the IC goes into normal operating mode, the frequency jittering is enabled. There is also frequency jittering during frequency reduction.

4.3.6 Modulated gate drive

The drive stage is optimized for EMI consideration. The switch-on speed is slowed down before it reaches the power MOSFET turn-on threshold. There is a slope control on the rising edge at the output of the driver (see Figure 13). In this way the leading switch spike during turn-on is minimized.

The gate drive is 10 V (V_{GATE_HIGH}), which is good enough for most of the available power MOSFETs. For a 1 nF load capacitance, the typical values of rise time and fall time are 117 ns and 27 ns respectively.

A gate resistor can be used to adjust the switch-on speed of the MOSFET. To speed up the switch-off, the gate resistor can be anti-paralleled with an ultrafast diode. To avoid the gate-drive oscillation on the power MOSFET, it is recommended to minimize the PCB loop. These suggestions are not applicable to CoolSET™, as the power MOSFET is already integrated with the controller and adjusted for optimized operation.

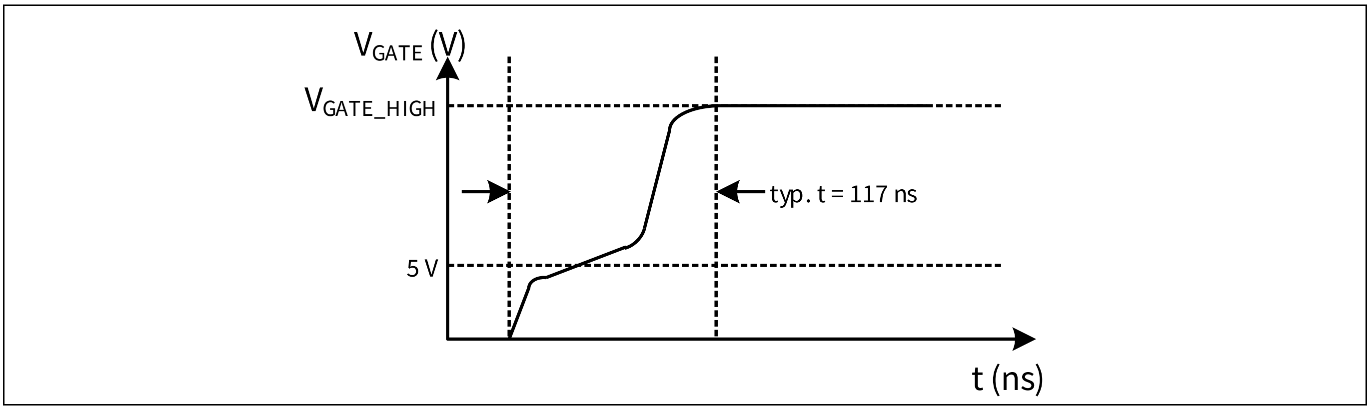

Figure 13 Gate – rising waveform

Attention: Do not add a gate discharge resistor on the gate of the power MOSFET or the GATE pin in ICE5xSAG/ICE5xRxxxxAG applications. The discharge resistor together with the $R_{StartUp}$ forms a voltage divider. With the high ratio of the resistance of $R_{StartUp}$ with discharge resistor, the gate voltage of the power MOSFET may not be enough turn it on and charge the V_{CC} to exceed V_{VCC_ON}. Similarly, connecting a voltage probe on the GATE pin even with CoolSET™ may result in a non-start-up or a longer start-up time, depending on the probe resistance.

4.4 Peak Current Limitation (PCL)

There is a cycle-by-cycle Peak Current Limitation (PCL) realized by the current limit comparator to provide primary Over Current Protection (OCP). The primary current generates a voltage V_{CS} across the CS resistor R_{CS} connected between the CS pin and the GND pin. If the voltage V_{CS} exceeds an internal voltage limit V_{CS_N}, the comparator immediately turns off the gate drive.

The primary peak current I_{PEAK_PRI} can be calculated as below:

$$I_{PEAK\_PRI} = V_{CS\_N}/R_{CS} \quad \text{(Eq 206)}$$

where I_{PEAK_PRI} : maximum peak current in the primary

V_{CS_N} : threshold voltage for the PCL

R_{CS} : resistance of the CS resistor

To avoid mis-triggering caused by MOSFET switch-on transient voltage spikes, a Leading Edge Blanking (LEB) time (t_{CS_LEB}) is integrated into the current sensing path.

Note: In case of high switch-on noise at the CS pin, the IC may switch off immediately after the LEB time, especially at light-load high-line conditions. To avoid this, a noise-filtering ceramic capacitor (e.g. 100 pF~100 nF) can be added across the CS pin and the GND pin.

4.4.1 Propagation delay compensation

In case of OC detection, there is always a propagation delay from sensing the V_{CS} to switching off the power MOSFET. An overshoot on the peak current I_{peak} caused by the delay depends on the ratio of dI/dt of the primary current (see Figure 14).

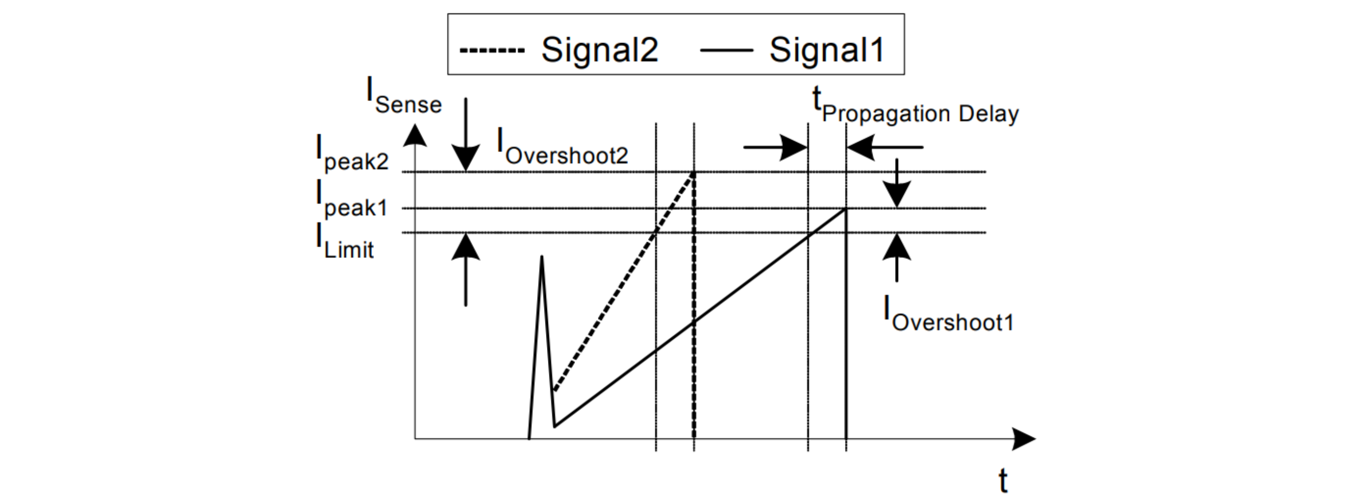

Figure 14 Current limiting

The overshoot of Signal2 is larger than Signal1 due to the steeper rising waveform. This change in the slope depends on the AC input voltage. Propagation delay compensation is integrated to reduce the overshoot due to dI/dt of the rising primary current. Thus the propagation delay time between exceeding the CS threshold V_{CS_N} and the switching off of the power MOSFET is compensated over a wide bus voltage range. Current limiting becomes more accurate, which will result in a minimum difference of over-load protection triggering power between low and high AC-line input voltage.

Under CCM operation, the same V_{CS} does not result in the same power. In order to achieve a close over-load triggering level for CCM, ICE5xSAG/ICE5xRxxxxAG has implemented a two-curve compensation, as shown in Figure 15. One of the curves is used for T_{ON} greater than 0.40 duty cycle and the other is for T_{ON} lower than 0.40 duty cycle.

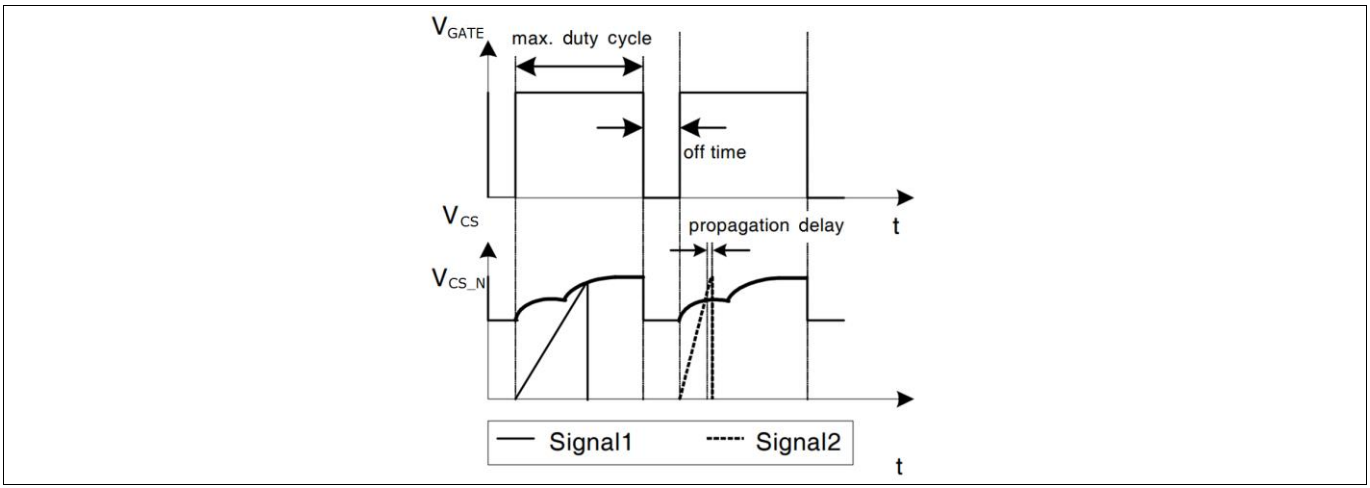

Figure 15 Dynamic voltage threshold V_{CS_N}

Similarly, the same concept of propagation delay compensation is also implemented in ABM at a reduced level. With this implementation, the entry and exit burst mode power can remain close between low and high AC-line input voltage.

4.5 ABM with selectable power level

At light load, the IC enters ABM operation to minimize power consumption. Details of ABM operation are explained in the following paragraphs.

4.5.1 Entering ABM operation

The system will enter ABM operation when two conditions are met:

- the FB voltage is lower than the threshold of V_{FB_EBLP}/V_{FB_EBHP} depending on burst configuration option set-up;
- and a certain blanking time t_{FB_BEB}.

Once both of these conditions are fulfilled, the ABM flip-flop is set and the controller enters ABM operation. This dual-condition determination for entering ABM operation prevents mis-triggering of ABM, so that the controller enters ABM operation only when the output power is really low.

The threshold power to enter burst mode can be determined using the equation below.

$$P_{\mathrm{enter\_burst}} = \frac{1}{2} \cdot L_p \cdot f_{OSCx\_MIN} \cdot \left(\frac{V_{FB\_EBxP} - V_{PWM}}{R_{CS} \cdot G_{PWM}}\right)^2 \qquad \textbf{(Eq 207)}$$

where L_P : primary inductance

f_{OSCx_MIN} : minimum switching frequency

V_{FB_EBxP} : V_{FB} entering ABM

The burst power as a ratio to the maximum input power P_{IN_Max} can be expressed in the equation below.

$$\frac{P_{enter\_burst}}{P_{IN\_Max}} = \frac{f_{OSCx\_MIN}}{f_{OSCx}} \cdot \left(\frac{V_{FB\_EBxP} - V_{PWM}}{V_{CS\_N} \cdot G_{PWM}}\right)^2 \qquad \textbf{(Eq 208)}$$

4.5.2 During ABM operation

After entering ABM, the PWM section will be inactive, making the V_{OUT} start to decrease. As the V_{OUT} decreases, V_{FB} rises. Once V_{FB} exceeds V_{FB_BOn}, the internal circuit is again activated by the internal bias to start the switching.

If the PWM is still operating and the output load is still low, V_{OUT} increases and the V_{FB} signal starts to decrease. When V_{FB} reaches the low threshold V_{FB_BOff}, the internal bias is reset again and the PWM section is disabled, with no switching until V_{FB} increases and once again exceeds the V_{FB_BOn} threshold.

In ABM, V_{FB} is like a sawtooth waveform swinging between V_{FB_BOff} and V_{FB_BOn}, as shown in Figure 16.

During ABM, the switching frequency f_{OSCx_ABM} is 83 kHz for the 100 kHz version and 103 kHz for the 125 kHz version of the IC. The peak current I_{PEAK_ABM} of the power MOSFET is defined by:

$$I_{\mathrm{PEAK\_ABM}} = V_{\mathrm{CS\_BxP}}/R_{\mathrm{CS}} \qquad \textbf{(Eq 209)}$$

where V_{CS_BxP} is the PCL in ABM

4.5.3 Leaving ABM operation

The FB voltage immediately increases if there is a sudden increase in the output load. When V_{FB} exceeds V_{FB_LB}, it will leave ABM and the PCL threshold voltage will return back to V_{CS_N} immediately.

The power on leaving ABM can be determined using the equation below.

$$P_{\text{leave\_}burst} = \frac{1}{2} \cdot L_p \cdot f_{OSCx\_ABM} \cdot \left(\frac{V_{CS\_BxP}}{R_{CS}}\right)^2 \quad \textbf{(Eq 210)}$$

where f_{OSCx_ABM} : ABM switching frequency

V_{CS_BxP} : PCL in ABM

Therefore, the ratio of the power on leaving ABM to maximum input power can be determined using the equation below.

$$\frac{P_{leave\_burst}}{P_{IN\_Max}} = \frac{f_{OSCx\_ABM}}{f_{OSCx}} \cdot \left(\frac{V_{CS\_BxP}}{V_{CS\_N}}\right)^2 \quad \textbf{(Eq 211)}$$

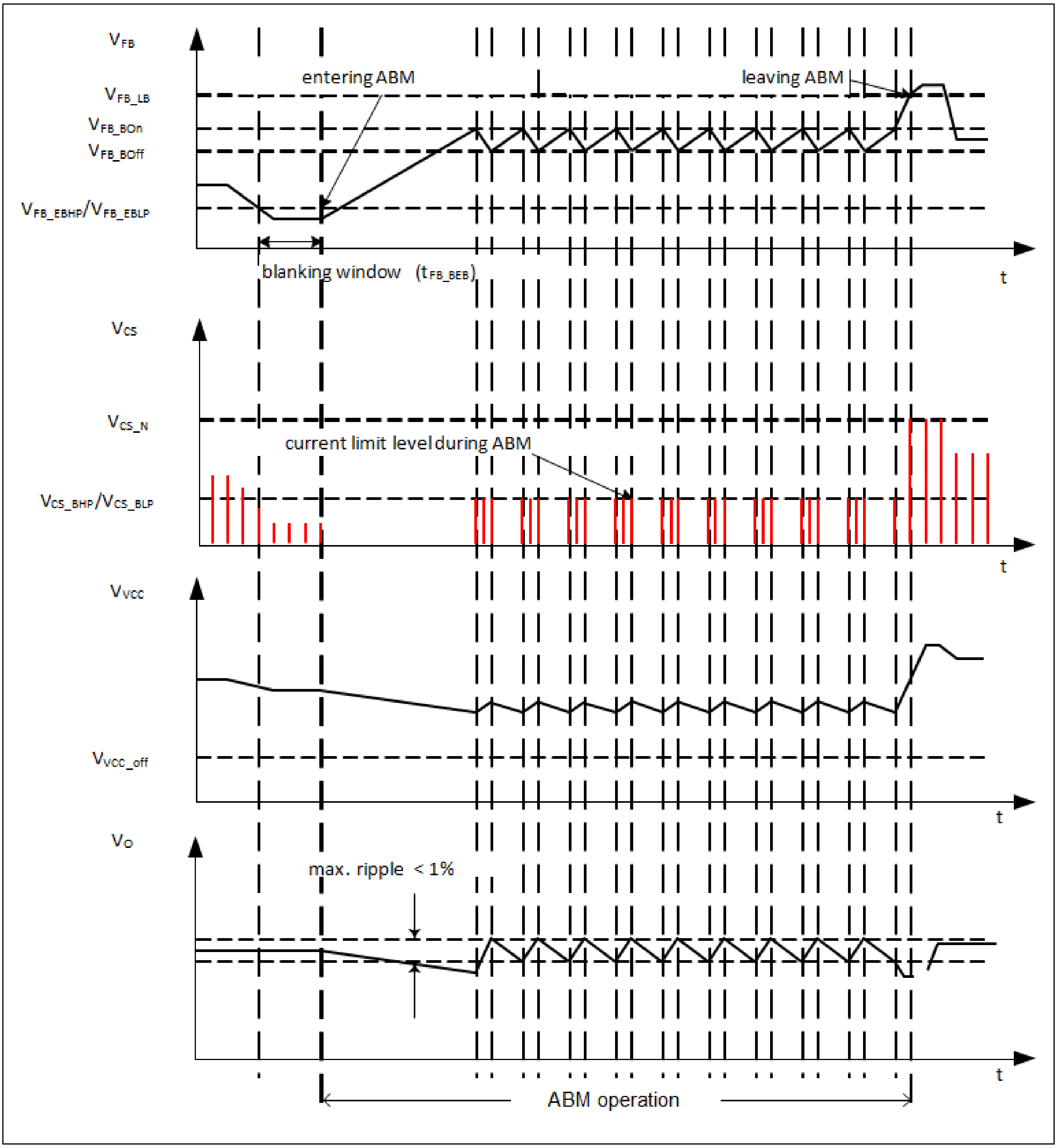

Figure 16 Signals in ABM

4.5.4 ABM configuration

The burst mode entry level can be selected by changing the resistance R_{Sel} at the FB pin. There are three configuration options depending on R_{Sel}, which corresponds to the options of no ABM (Option 1), low range of ABM power (Option 2) and high range of ABM power (Option 3). The table below shows the control logic for the entry and exit levels with the FB voltage.

Table 2 ABM configuration option set-up

Option	R_{Sel}	V_{FB}	V_{CS_BxP}	Entry level		Exit level	
				V_{FB_EBxP}	Percentage of P_{IN_Max}	V_{FB_LB}	Percentage of P_{IN_Max}
1	< 470 kΩ	$V_{FB} < V_{FB\_P\_BIAS1}$	–	–	No ABM	–	No ABM
2	720~790 kΩ	$V_{FB\_P\_BIAS1} < V_{FB} < V_{FB\_P\_BIAS2}$	0.22 V	0.93 V	~3 %	2.73 V	~6.2 %
3 (default)	> 1210 kΩ	$V_{FB} > V_{FB\_P\_BIAS2}$	0.27 V	1.03 V	~4.5 %	2.73 V	~9.4 %

P_{IN_Max} is the input power before the over-load protection is triggered.

During start-up of the IC, the controller presets the ABM selection to Option 3, the FB resistor (R_{FB}) is turned off by internal switch S2 (see Figure 17) and a current source I_{sel} is turned on instead. From V_{CC} = 4.44 V to the V_{CC} on-threshold, the FB pin will start to charge resistor R_{Sel} with current I_{Sel} to a certain voltage level. When V_{CC} reaches the V_{CC} on-threshold, the FB voltage is sensed. The burst mode option is then chosen according to the FB voltage level. After finishing the selection, any change on the FB level will not change the burst mode option, and the current source (I_{sel}) is turned off while the FB resistor (R_{FB}) is connected back to the circuit.

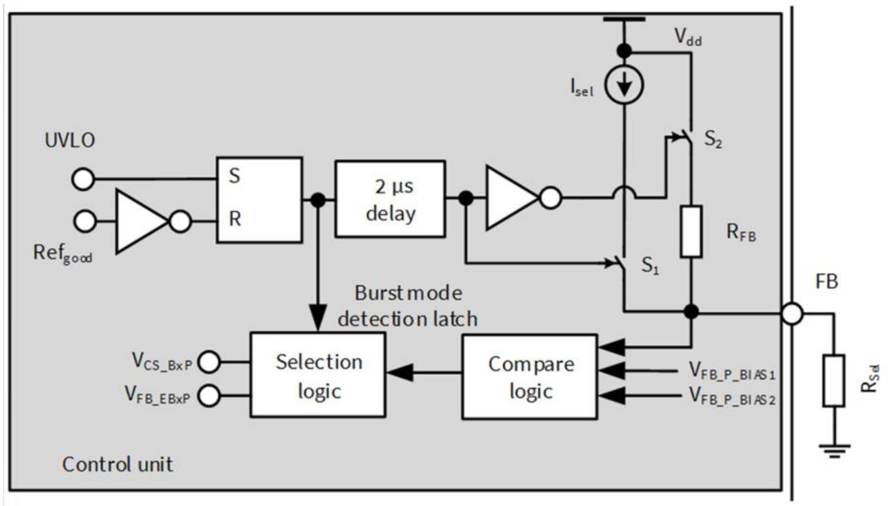

Figure 17 ABM detect and adjust

4.6 Non-isolated/isolated configuration

ICE5xSAG/ICE5xRxxxxAG has a VERR pin, which is connected to the input of an integrated error amplifier to support non-isolated Flyback application (see Figure 4 and Figure 5). When the V_{CC} is charging and before reaching the V_{CC} on-threshold, a current source $I_{ERR\_P\_BIAS}$ from the VERR pin together with R_{F1} and R_{F2} will generate a voltage across it. If the VERR voltage is more than $V_{ERR\_P\_BIAS}$ (0.2 V), non-isolated configuration is selected; otherwise, isolated configuration is selected. In isolated configuration, the error amplifier output is disconnected from the FB pin.

Connect the VERR pin to GND if an error amplifier is not used or if isolated configuration is selected.

4.6.1 Non-isolated FB

In case of non-isolated configuration (refer to Figure 4 and Figure 5), the voltage divider R_{F1} and R_{F2} is used to sense the output voltage and compared with the internal reference voltage V_{ERR_REF}. The difference between the sensed voltage and the reference voltage is converted as an output current by the error amplifier. The output current will charge/discharge the resistor and capacitor network connected at the FB pin for the loop compensation.

To properly detect a non-isolated configuration, the minimum resistance for the parallel combination of resistors R_{F1} and R_{F2} is calculated below:

$$R_{F1//F2} \geq V_{ERR\_P\_BIAS\_max}/I_{ERR\_P\_BIAS\_min} = 0.24V/9.5\mu A = 25.3\ k\Omega \quad \text{(Eq 212)}$$

where $R_{F1//F2}$: parallel combination of R_{F1} and R_{F2}

$V_{ERR\_P\_BIAS\_max}$: maximum voltage for error amplifier mode

$I_{ERR\_P\_BIAS\_min}$: minimum bias current for error amplifier mode

The output voltage V_{P1} (see Figure 4) is set by R_{F1} and R_{F2} using the equation below:

$$R_{F2} = R_{F1} \cdot \left(\frac{V_{P1}}{V_{ERR\_REF}} - 1\right) \quad \text{(Eq 213)}$$

where R_{F1} and R_{F2} : voltage divider resistors

V_{P1} : output voltage

V_{ERR_REF} : error amplifier reference voltage

4.6.2 Isolated FB

In isolated configuration, the output is usually sensed by a TL431, and the output is fed to the FB pin by the optocoupler (see Figure 18). Inside the IC, the FB pin is connected to a (V_{REF}) 3.3 V reference voltage through an internal pull-up resistor R_{FB}. Outside the IC, this pin is connected to the collector of the optocoupler. Normally, a ceramic capacitor C_{FB}, e.g. 1 nF, can be placed between this pin and GND to filter out noise.

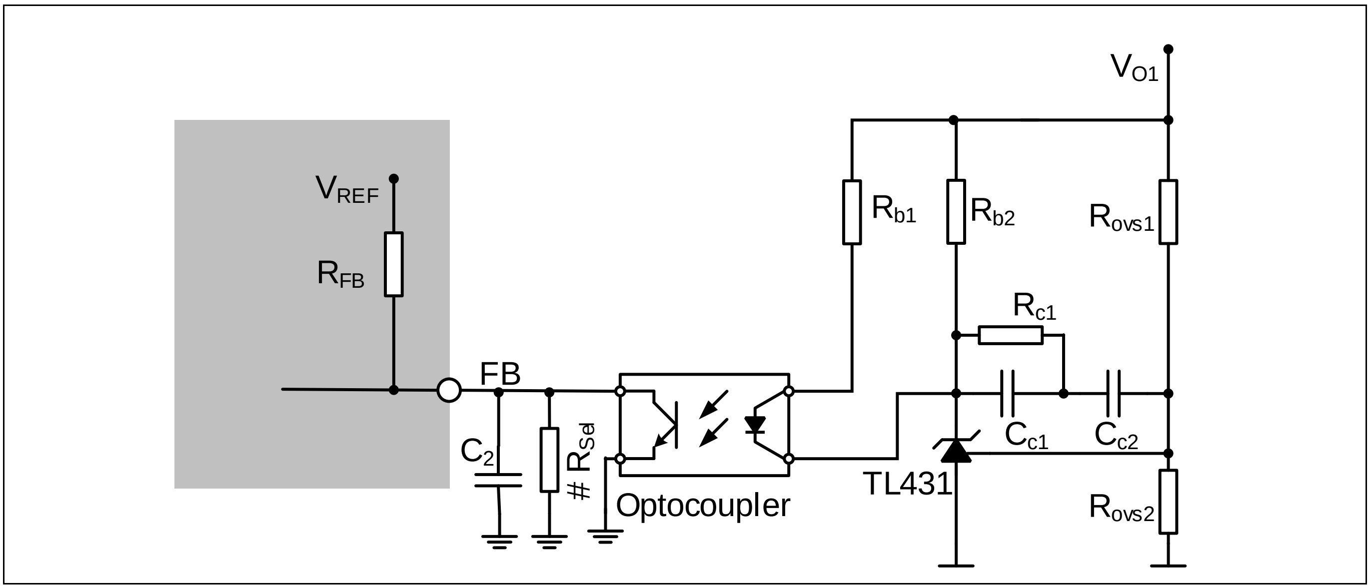

Figure 18 FB circuit for isolated configuration

The output voltage V_{O1} (see Figure 18) is set by R_{OVS1} and R_{OVS2} using the equation below:

$$R_{OVS1} = R_{OVS2}\left(\frac{V_{O1}}{V_{REF\_TL}} - 1\right) \quad \text{(Eq 214)}$$

where R_{OVS1} and R_{OVS2} : voltage divider resistors

V_{O1} : output voltage

V_{REF_TL} : TL431 reference voltage

4.7 Protection functions

The ICE5xSAG/ICE5xRxxxxAG provides numerous protection functions that considerably improve the power supply system robustness, safety and reliability. The following table summarizes these protection functions and the corresponding protection mode, whether non-switch auto-restart, auto-restart or odd-skip auto-restart. Refer to Figure 19, Figure 20 and Figure 21 for the waveform illustration of the protection modes.

Table 3 Protection functions

Protection functions	Normal mode	Burst mode		Protection mode
		Burst ON	Burst OFF	
LOVP	√	√	√	Non-switch auto-restart
V_{CC} OV	√	√	NA[1]	Odd-skip auto-restart
V_{CC} UV	√	√	√	Auto-restart
Over-load/open-loop	√	NA[1]	NA[1]	Odd-skip auto-restart
Over-temperature	√	√	√	Non-switch auto-restart
CS short-to-GND	√	√	NA[1]	Odd-skip auto-restart
V_{CC} short to GNDshort-to-GND	√	√	√	No start-up

4.7.1 LOVP

The input LOVP is detected by sensing the bus capacitor voltage through the VIN pin via voltage divider resistors R_{I1} and R_{I2} (Figure 2). Once the V_{VIN} voltage is higher than the the LOV threshold (V_{VIN_LOVP}), the controller enters protection mode until V_{VIN} is lower than V_{VIN_LOVP}. This protection can be disabled by connecting the VIN pin to GND.

During LOVP, there is no MOSFET switching and V_{VIN} is always monitored in every restart cycle. The sensing resistors (see Figure 2, Figure 3, Figure 4 and Figure 5) R_{I1} and R_{I2} can be calculated as in the equation below.

$$R_{I2} = \frac{R_{I1} \times V_{VIN\_LOVP}}{(V_{Line\_OVP\_AC} \times \sqrt{2}) - V_{VIN\_LOVP}} \quad \textbf{(Eq 215)}$$

where R_{I1} : high-side line input sensing resistor (typ. 9 MΩ)

R_{I2} : low-side line input sensing resistor

V_{VIN_LOVP} : LOV threshold (typ. 2.85 V)

$V_{LINE\_OVP\_AC}$: user-defined LOV (V_{AC}) for the system

[1] Not applicable

4.7.2 V_{CC} OV/UV

During operation, the V_{CC} voltage is continuously monitored. If V_{CC} is either below V_{VCC_OFF} for 50 µs ($t_{VCC\_OFF\_B}$) or above V_{VCC_OVP} for 55 µs ($t_{VCC\_OVP\_B}$), the power MOSFET is kept switched off. After the V_{CC} voltage falls below the threshold V_{VCCoff}, the new start-up sequence is activated. The V_{CC} capacitor is then charged up. Once the voltage exceeds the threshold V_{VCC_ON}, the IC begins to operate with a new soft-start.

4.7.3 Over-load/open-loop

In case of open control-loop or output over-load, the FB voltage will be pulled up. When V_{FB} exceeds V_{FB_OLP} after a blanking time of $t_{FB\_OLP\_B}$, the IC enters odd-skip auto-restart mode. The blanking time enables the converter to provide peak power in case the increase in V_{FB} is due to a sudden load increase.

4.7.4 Over-temperature

If the junction temperature of the controller exceeds T_{jcon_OTP}, the IC enters Over Temperature Protection (OTP) in auto-restart mode. The IC is also implemented with a 40°C hysteresis. That means the IC can only be recovered from OTP when the controller junction temperature drops 40°C lower than the OT trigger point.

4.7.5 CS short-to-GND

If the voltage at the CS pin is lower than the preset threshold V_{CS_STG} with a certain blanking time $t_{CS\_STG\_B}$ for three consecutive pulses during the on-time of the power switch, the IC enters CS short-to-GND protection.

4.7.6 V_{CC} short-to-GND

To limit the power dissipation of the start-up circuit at V_{CC} short-to-GND, the V_{CC} charging current is limited to a minimum level of $I_{VCC\_Charge1}$. With such low current, the power loss of the IC is limited to prevent over-heating.

4.7.7 Protection modes

All the protections are in auto-restart mode with a new soft-start sequence. The three auto-restart modes are illustrated in the following figures.

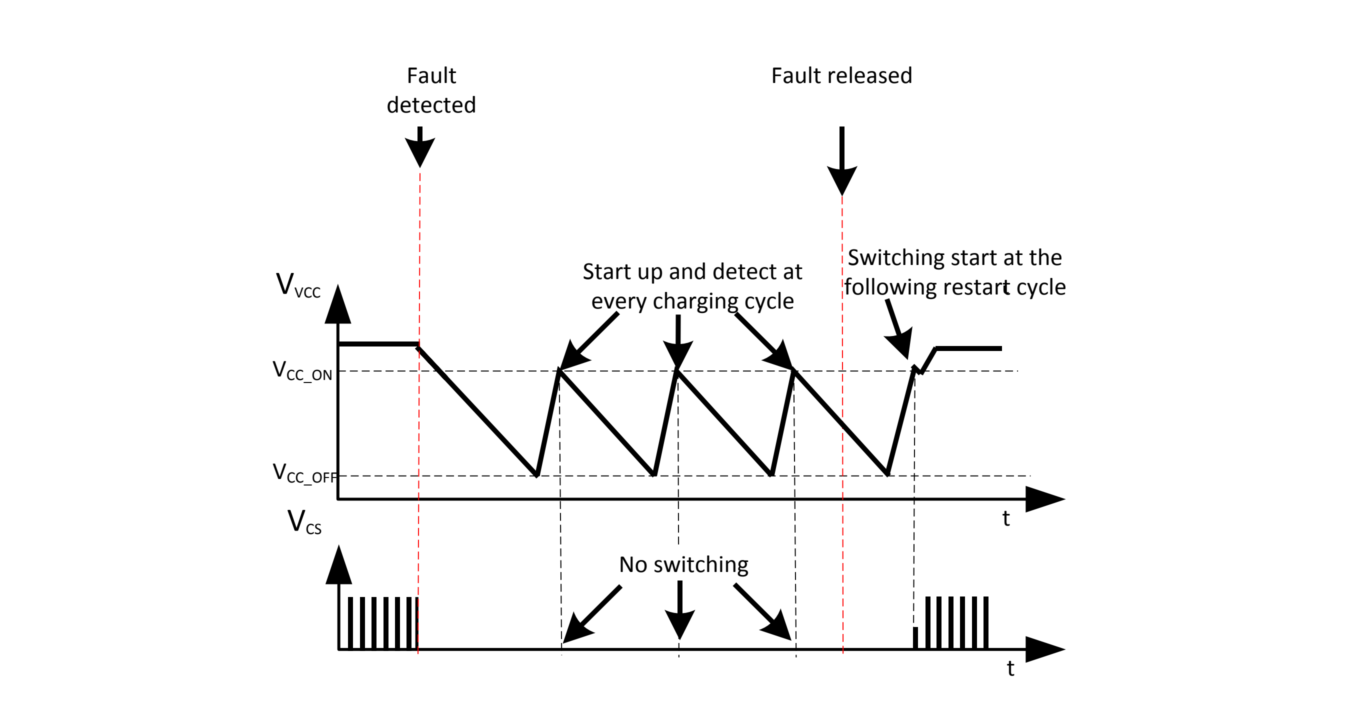

Figure 19 Non-switch auto-restart mode

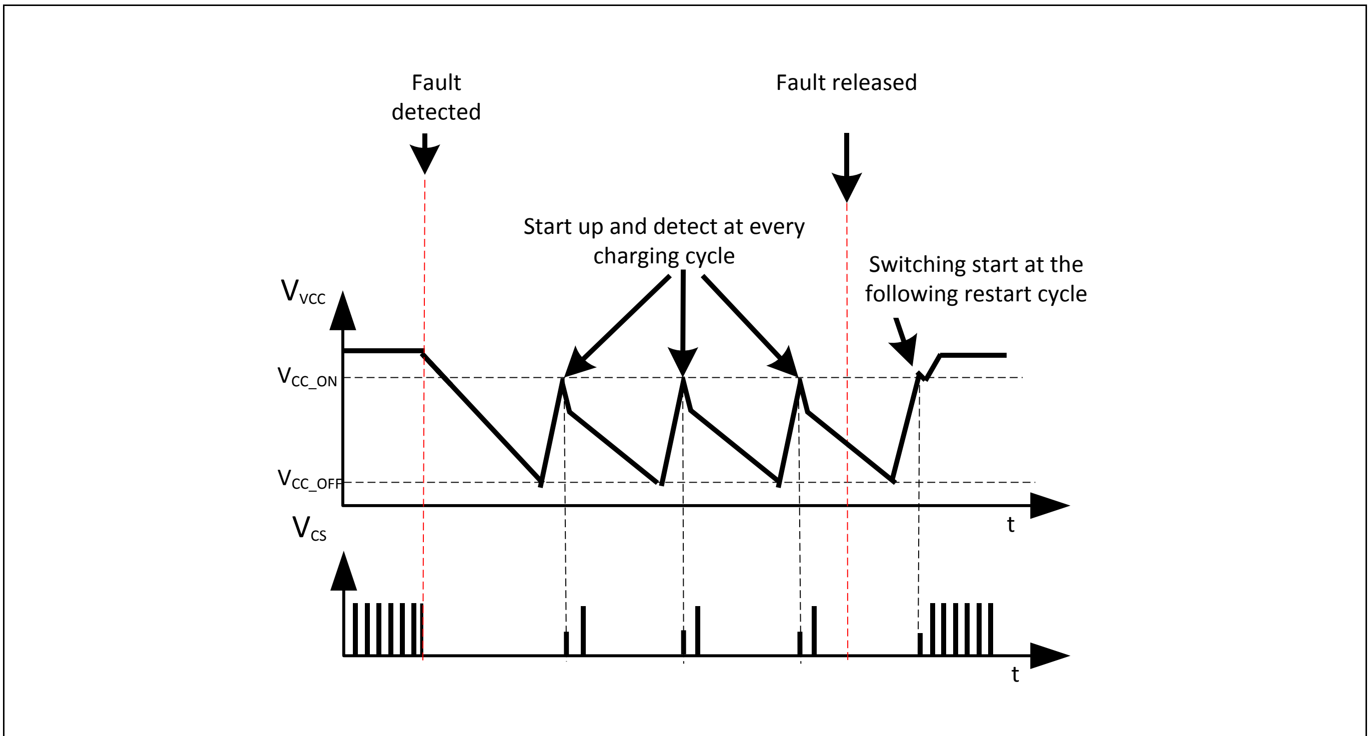

Figure 20 Auto-restart mode

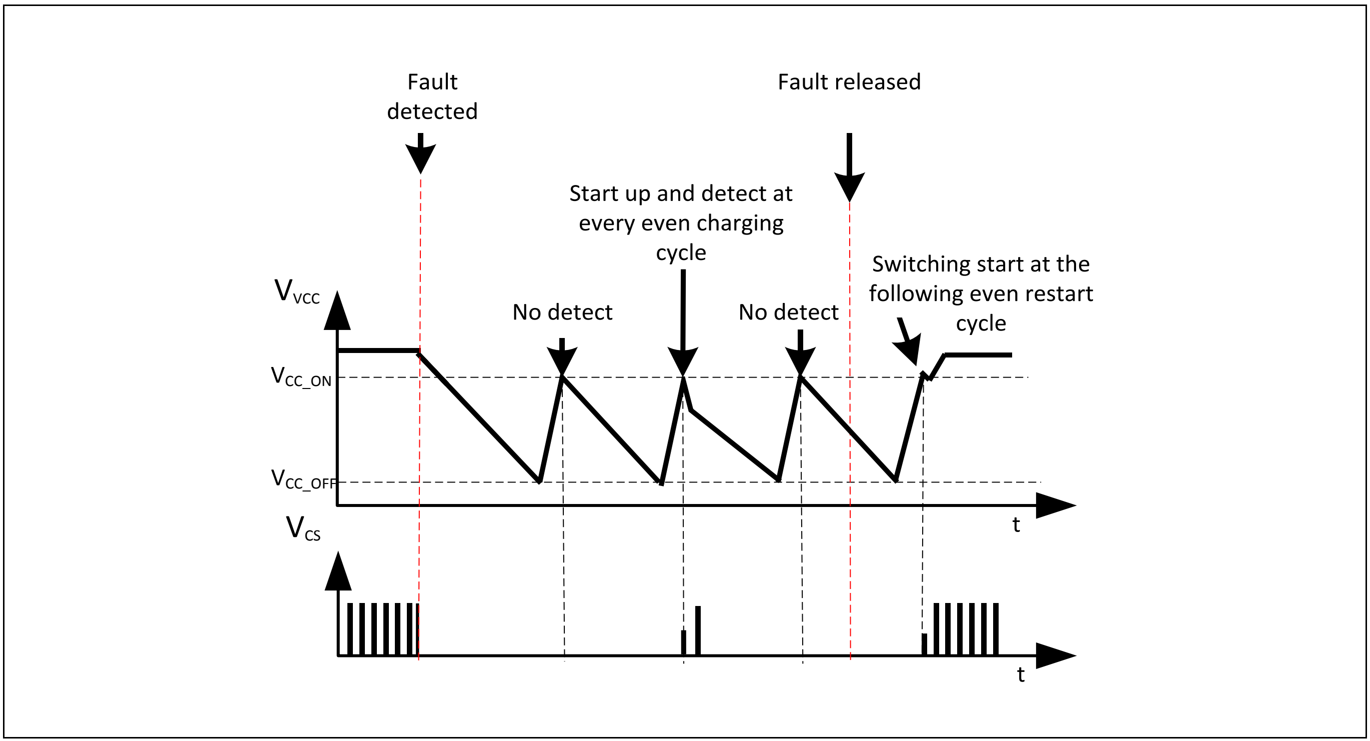

Figure 21 Odd-skip auto-restart

5 Typical application circuit

A 60 W single-output demo board with ICE5GSAG and 14.5 W demo board with ICE5AR4770AG are shown below.

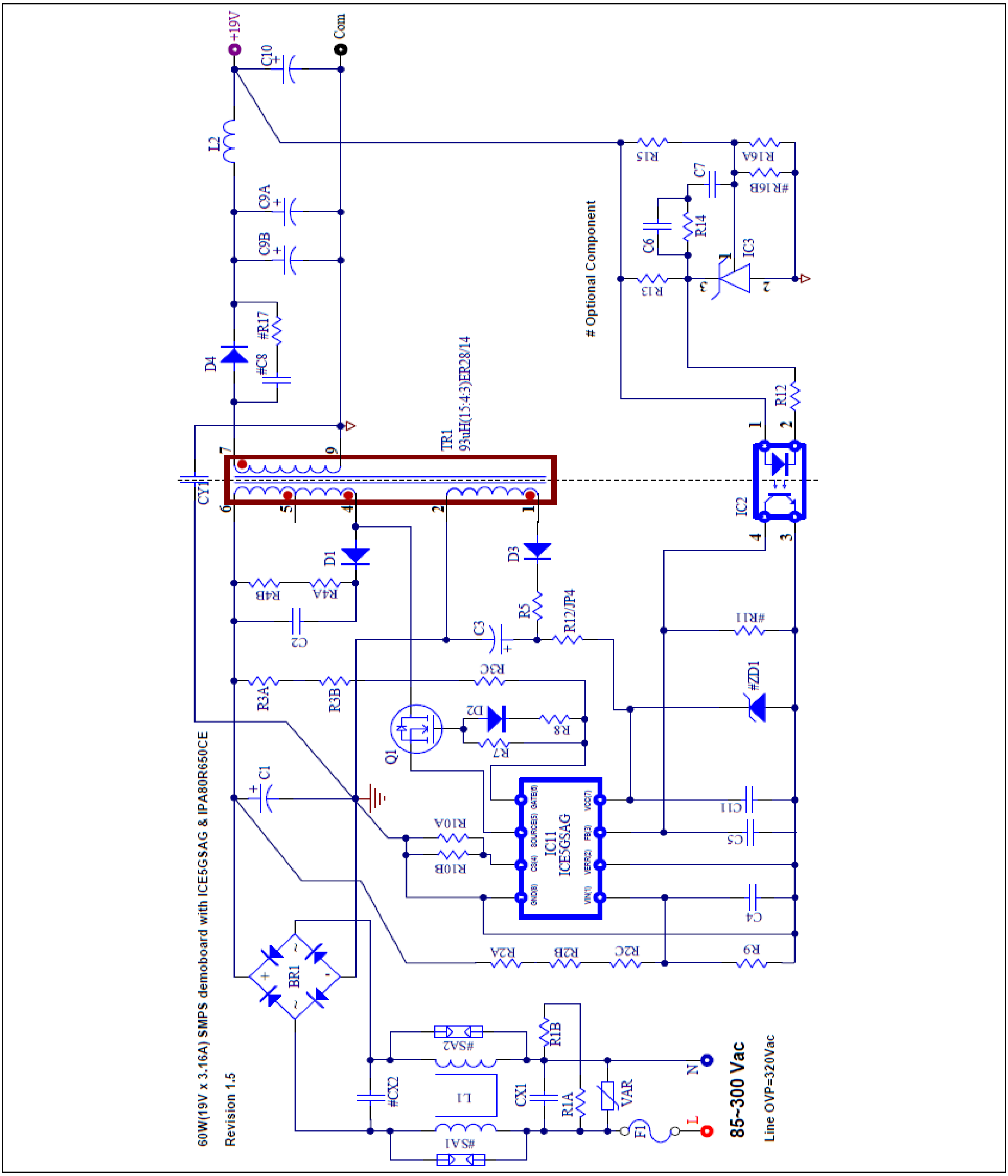

Figure 22 Schematic of DEMO_5GSAG_60W1

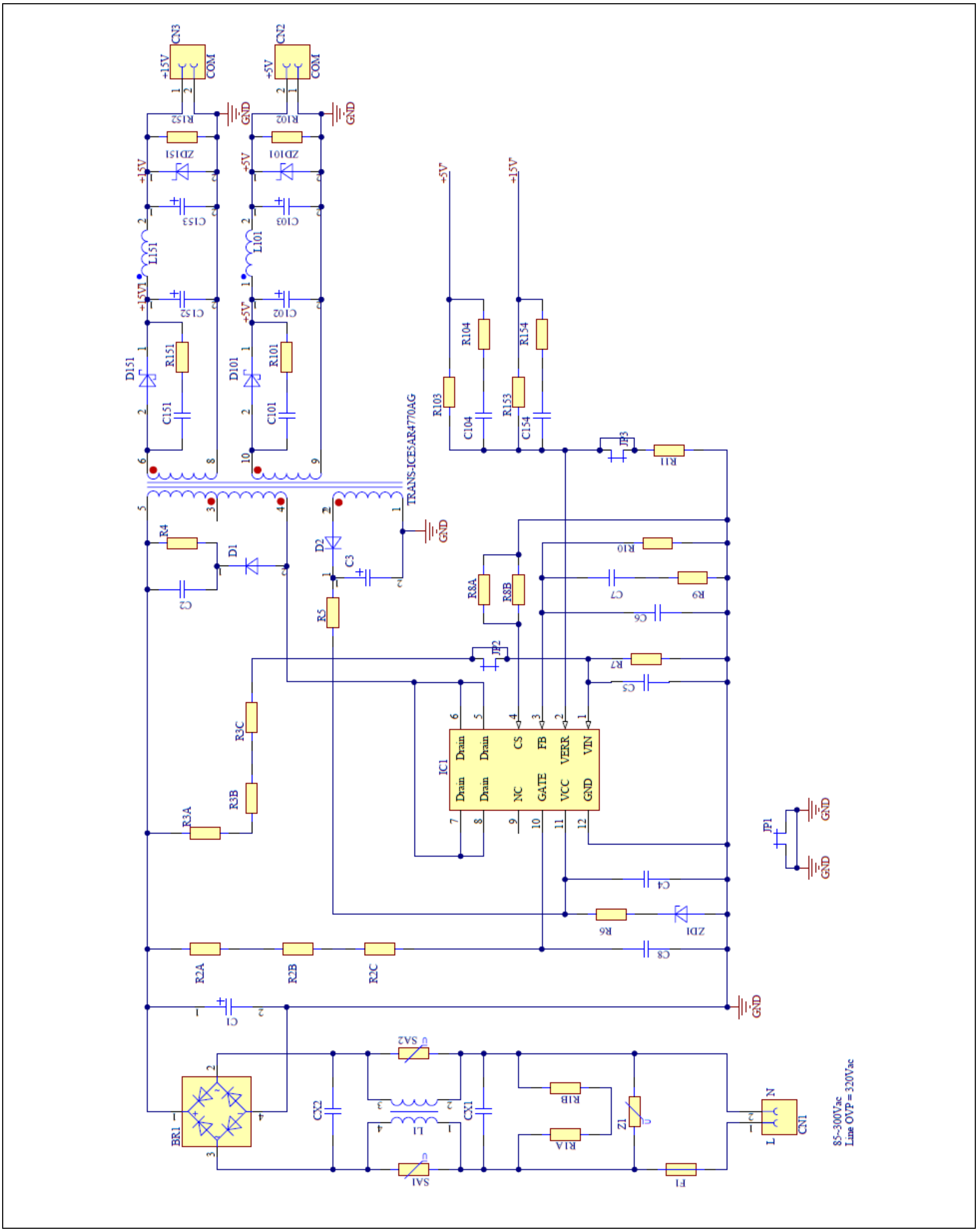

Figure 23 Schematic of DEMO_5AR4770AG_14W1

6 PCB layout recommendation

In an SMPS, the PCB layout is crucial to a successful design. Below are some recommendations (see Figure 22).

1. Minimize the loop with pulse share current or voltage; examples are the loop formed by the bus voltage source, primary winding, main power switch (Q1 in the controller or power switch CoolMOS™ inside the CoolSET™) and CS resistor or the loop consisting of the secondary winding, output diode and output capacitor, or the loop of the V_{CC} power supply.
2. Star the ground at the bulk capacitor C1: all primary grounds should be connected to the ground of the bulk capacitor C1 separately at one point. This can reduce the switching noise entering the sensitive pins of the CoolSET™ device. The primary star ground can be split into four groups as follows:
   i. Combine signal (all small-signal grounds connecting to the controller/CoolSET™ GND pin such as the filter capacitor ground C4, C5, C11 and optocoupler ground) and power ground (CS resistor R10A and R10B).
   ii. V_{CC} ground includes the V_{CC} capacitor C3 ground and the auxiliary winding ground, pin 2 of the power transformer.
   iii. EMI return ground includes the Y capacitor CY1.
   iv. DC ground from the bridge rectifier BR1.
3. Place the filter capacitor close to the controller ground: filter capacitors C4, C5 and C11 should be placed as close to the controller ground and the controller pin as possible so as to reduce the switching noise coupled into the controller.
4. HV traces clearance: HV traces should maintain sufficient spacing to the nearby traces. Otherwise, arcing could occur.
   i. 400 V traces (positive rail of bulk capacitor C1) to nearby traces: > 2.0 mm
   ii. 700/800 V traces {drain pin of power switch (Q1 in the controller and DRAIN pin of CoolSET™ IC1 [see Figure 23])} to nearby traces: > 3 mm
5. Recommended minimum of 232 mm^2 copper area at the DRAIN pin to add to the PCB for better thermal performance of the CoolSET™.

7 Output power of fifth-generation fixed-frequency ICs

Table 4 Output power of fifth-generation fixed-frequency controller

Type	Package	Marking	f_{sw}	220 V AC ±20 % at DCM[1]	85–300 V AC at DCM[1]	85–300 V AC at CCM[1]
ICE5ASAG	PG-DSO-8	5ASAG	100 kHz	108 W	60 W	66 W
ICE5GSAG	PG-DSO-8	5GSAG	125 kHz	108 W	60 W	66 W

Table 5 Output power of fifth-generation fixed-frequency CoolSET™

Type	Package	Marking	V_{DS}	f_{sw}	R_{DSon}[2]	220 V AC ±20 % at DCM[1]	85–300 V AC at DCM[1]	85–300 V AC at CCM[1]
ICE5AR4770AG	PG-DSO-12	5AR4770AG	700 V	100 kHz	4.73 Ω	27 W	15 W	16 W
ICE5GR4780AG	PG-DSO-12	5GR4780AG	800 V	125 kHz	4.13 Ω	27.5 W	15 W	16 W
ICE5GR2280AG	PG-DSO-12	5GR2280AG	800 V	125 kHz	2.13 Ω	41 W	23 W	24 W
ICE5GR1680AG	PG-DSO-12	5GR1680AG	800 V	125 kHz	1.53 Ω	48 W	27 W	28 W
ICE5AR0680AG	PG-DSO-12	5AR0680AG	800 V	100 kHz	0.71 Ω	68 W	40 W	42 W

The calculated output power curves showing typical output power against ambient temperature are shown below. The curves are derived based on an open-frame design at T_a = 50°C, T_J = 125°C (integrated HV MOSFET for CoolSET™), using the minimum pin copper area in a 2 oz copper single-sided PCB and steady-state operation only (no design margins for abnormal operation modes are included). The output power figure is for selection purposes only. The actual power can vary depending on the specific design.

[1] Calculated maximum output power rating in an open-frame design at T_a = 50°C, T_J = 125°C using minimum pin copper area in a 2 oz copper single-sided PCB. The output power figure is for selection purposes only. The actual power can vary depending on the particular design. Please contact a technical expert from Infineon for more information.

[2] Typ. at T_J = 25°C (inclusive of low-side MOSFET)

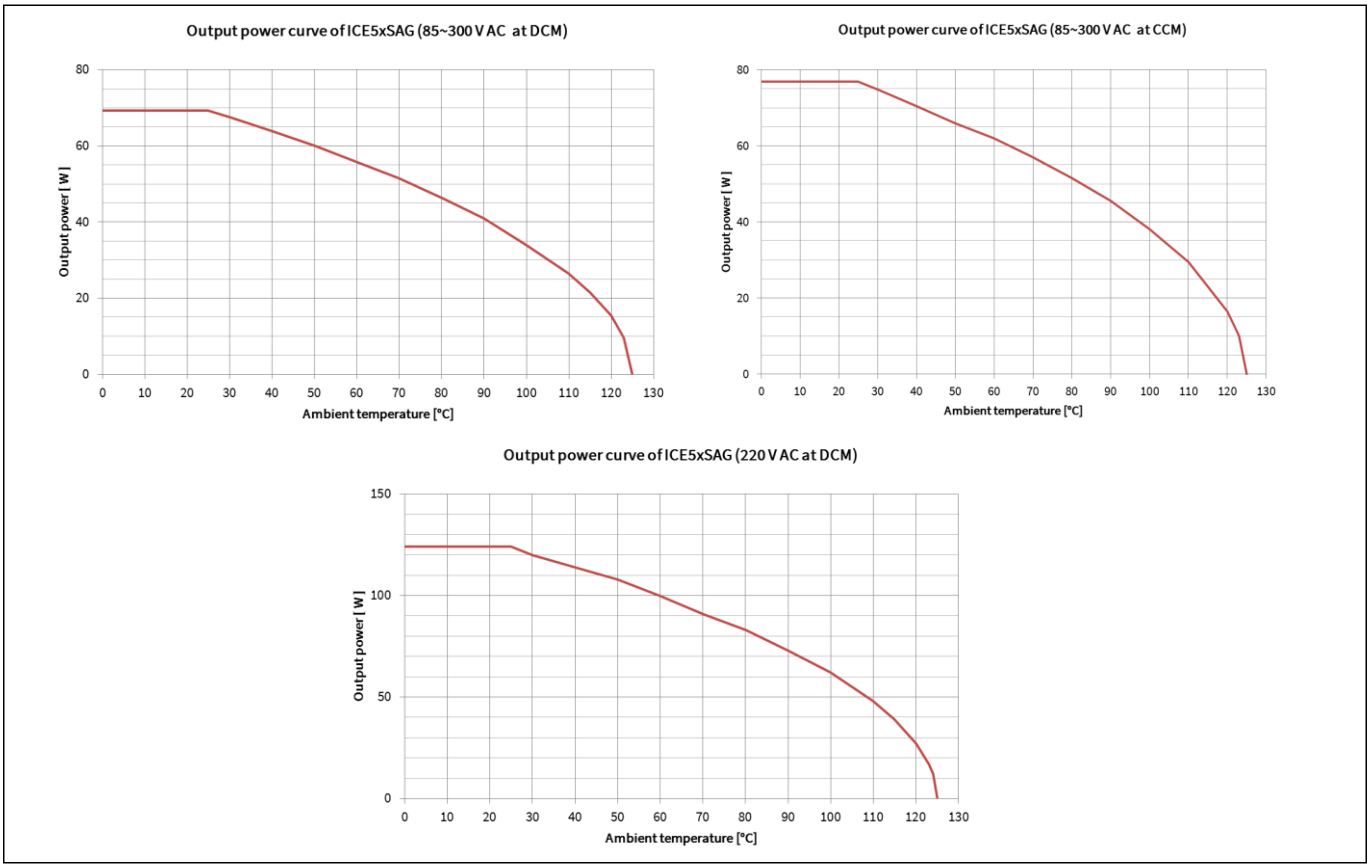

Figure 24 Output power curve of ICE5xSAG

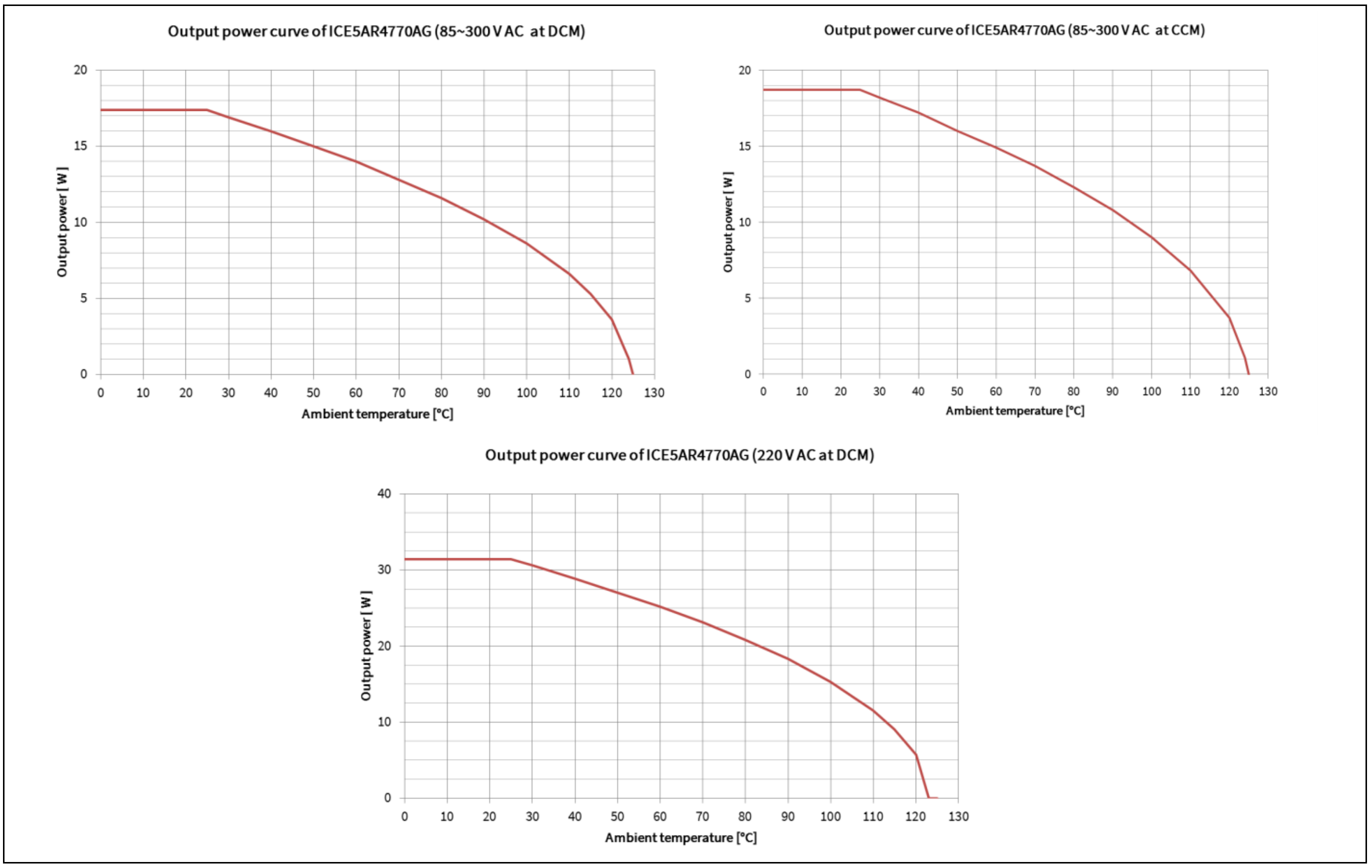

Figure 25 Output power curve of ICE5AR4770AG

Output power of fifth-generation fixed-frequency ICs

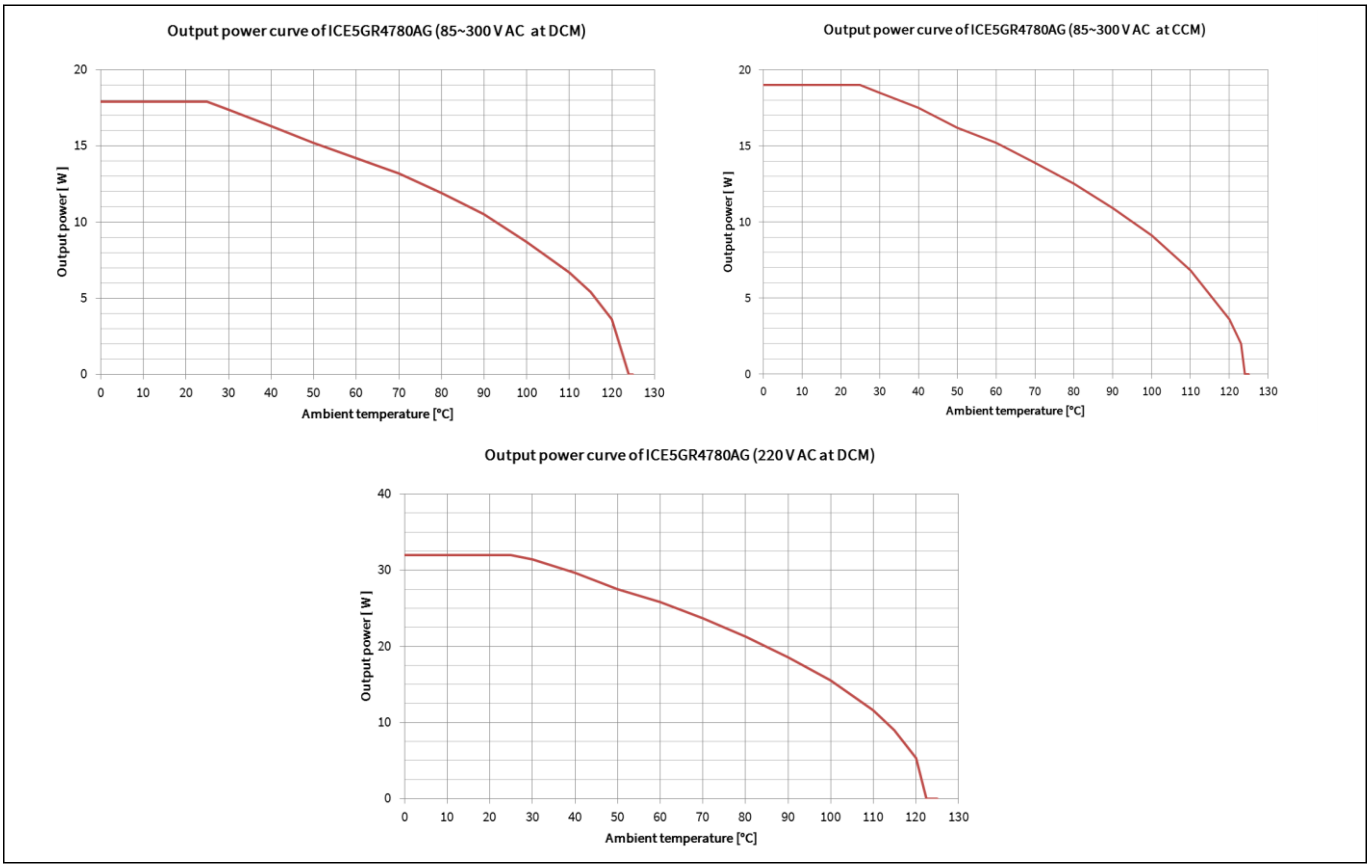

Figure 26 Output power curve of ICE5GR4780AG

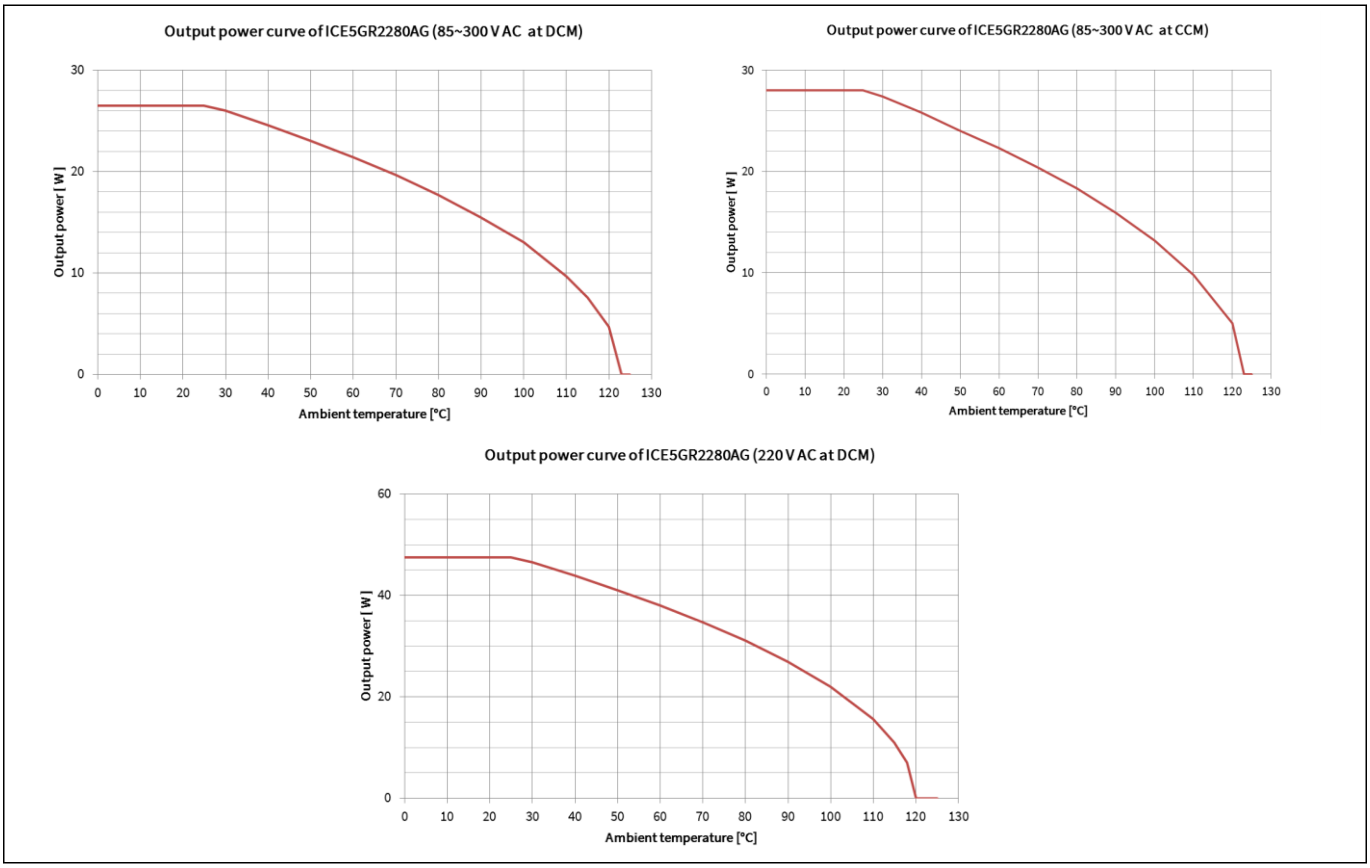

Figure 27 Output power curve of ICE5GR2280AG

Output power of fifth-generation fixed-frequency ICs

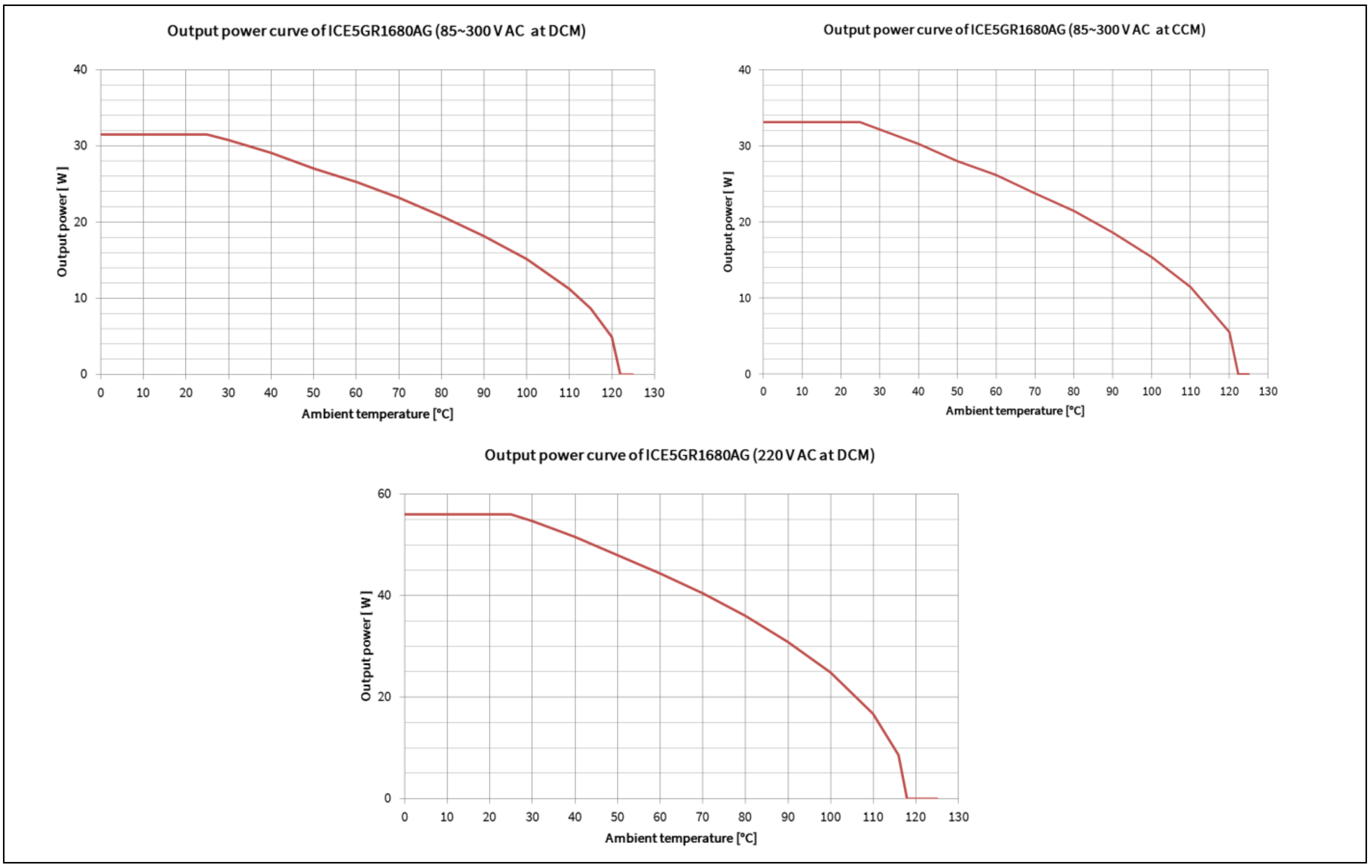

Figure 28 Output power curve of ICE5GR1680AG

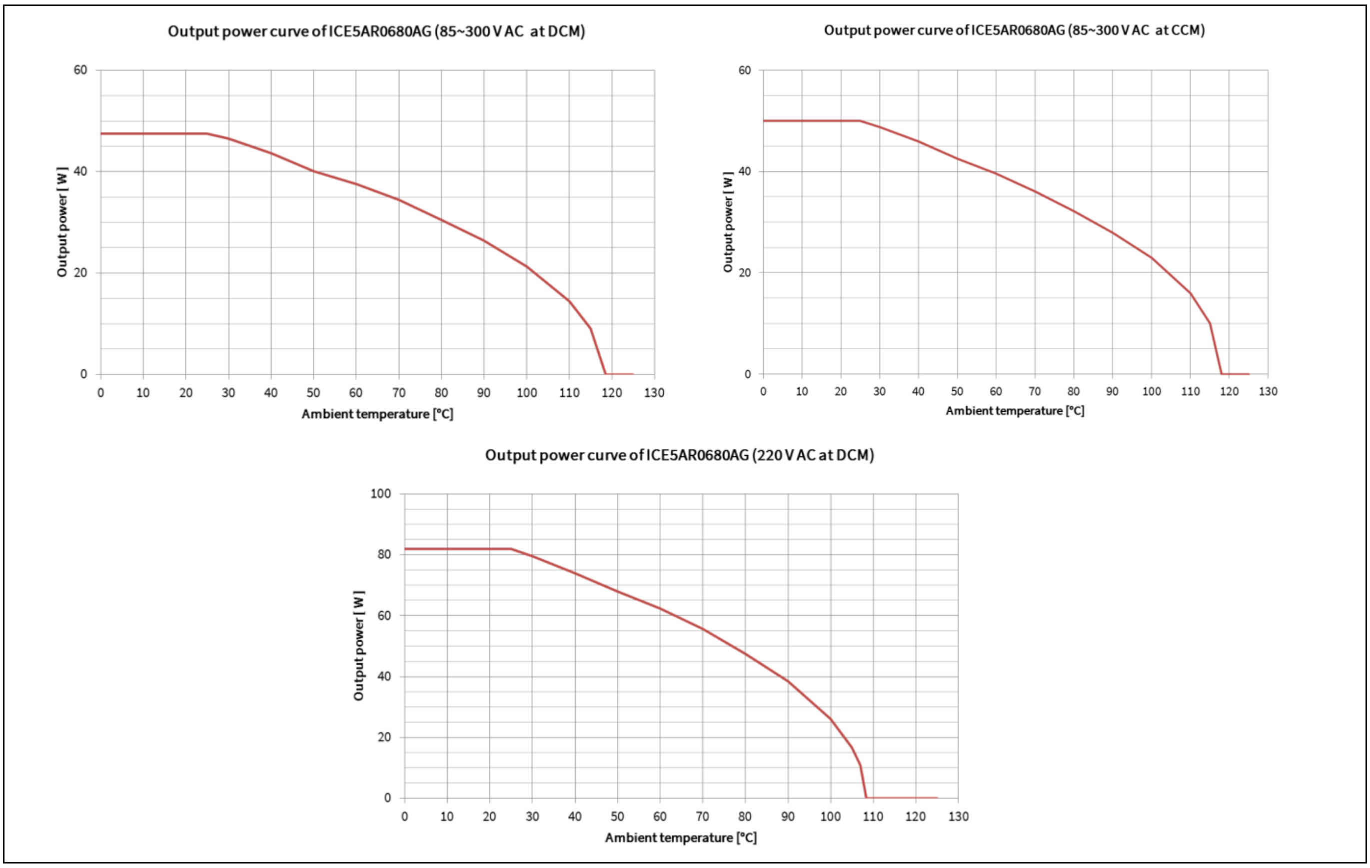

Figure 29 Output power curve of ICE5AR0680AG

8 Fifth-generation fixed-frequency FLYCAL design example

A design example of a 14.5 W 15 V 5 V fixed-frequency non-isolated DCM Flyback converter with ICE5AR4770AG is shown below.

Define input parameters:		
Minimum AC input voltage:	V_{ACMin}	85 V AC
Maximum AC input voltage:	V_{ACMax}	330 V AC
Line frequency:	f_{AC}	60 Hz
Bulk capacitor DC ripple voltage:	$V_{DCRipple}$	27 V
Output voltage 1:	V_{Out1}	15 V
Output current 1:	I_{Out1}	0.83 A
Forward voltage of output diode 2:	V_{FOut1}	0.6 V
Output ripple voltage 1:	$V_{OutRipple1}$	0.2 V
Output voltage 2:	V_{Out2}	5 V
Output current 2:	I_{Out2}	0.4 A
Forward voltage of output diode 2:	V_{FOut2}	0.2 V
Output ripple voltage 2:	$V_{OutRipple2}$	0.2 V
Maximum output power:	P_{OutMax}	17 W
Minimum output power:	P_{OutMin}	1 W
Efficiency at V_{ACMin} and P_{OutMax}:	η	83 %
Reflection voltage:	V_{RSET}	97.5 V
V_{CC} voltage:	V_{Vcc}	14 V
Forward voltage of V_{CC} diode (D2):	V_{FVcc}	0.6 V
Fifth-generation FF CoolSET™:	CoolSET™	ICE5AR4770AG
Switching frequency:	f_s	100 kHz
Breakdown voltage:	V_{DSMax}	700 V
Drain-to-source capacitance of MOSFET (including $C_{o(er)}$ of MOSFET):	C_{DS}	7 pF
Effective output capacitance of MOSFET:	$C_{O(er)}$	3.4 pF
Start-up resistor $R_{StartUp}$ (R2A, R2B, R2C):	$R_{StartUp}$	45 MΩ
Maximum ambient temperature:	T_a	50 °C

8.1 Pre-calculation

Output power of output 1:

$$P_{Out1} = V_{Out1} \cdot I_{Out1} \quad \textbf{(Eq 001)} \quad P_{Out1} = 15V \cdot 0.83A = 12.45W$$

Output power of output 2:

$$P_{Out2} = V_{Out2} \cdot I_{Out2} \quad \textbf{(Eq 002)} \quad P_{Out2} = 5V \cdot 0.4A = 2W$$

Nominal output power:

$$P_{OutNom} = P_{Out1} + P_{Out2} \quad \textbf{(Eq 003)} \quad P_{OutNom} = 12.45W + 2W = 14.45W$$

Output power 1 load weight:

$$K_{L1} = P_{Out1} / P_{OutNom}$$ (Eq 004) $$K_{L1} = 12.45W / 14.45W = 0.86$$

Output power 2 load weight:

$$K_{L2} = P_{Out2} / P_{OutNom}$$ (Eq 005) $$K_{L1} = 2W / 14.45W = 0.14$$

Maximum input power:

$$P_{InMax} = \frac{P_{OutMax}}{\eta}$$ (Eq 006) $$P_{InMax} = \frac{17W}{0.83} = 20.48W$$

8.2 Input diode bridge (BR1)

Input RMS current:

Power factor cosφ 0.6

$$I_{ACRMS} = \frac{P_{InMax}}{V_{ACMin} \cdot \cos\varphi}$$ (Eq 007) $$I_{ACRMS} = \frac{20.48W}{85V \cdot 0.6} = 0.402A$$

Maximum DC input voltage:

$$V_{DC\max PK} = V_{ACMax} \cdot \sqrt{2}$$ (Eq 008) $$V_{DCMaxPk} = 330V \cdot \sqrt{2} = 466.7V$$

8.3 Input capacitor (C1)

Peak voltage at minimum AC input:

$$V_{DCMinPk} = V_{ACMin} \cdot \sqrt{2}$$ (Eq 009) $$V_{DCMinPk} = 85V \cdot \sqrt{2} = 120.2V$$

Minimum DC input voltage-based ripple voltage setting:

$$V_{DCMinSet} = V_{DCMinPk} - V_{DCRipple}$$ (Eq 010) $$V_{DCMin}Set = 120.2V - 27V = 93.2V$$

Discharging time at each half-line cycle:

$$T_D = \frac{1}{4 \cdot f_{AC}} \cdot \left(1 + \frac{\sin^{-1} \frac{V_{DCMinSet}}{V_{DCMinPk}}}{90} \right)$$ (Eq 011) $$T_D = \frac{1}{4 \cdot 60Hz} \cdot \left(1 + \frac{\sin^{-1} \frac{93.2V}{120.2V}}{90} \right) = 6.52ms$$

Required energy at discharging time of input capacitor:

$$W_{IN} = P_{INMax} \cdot T_D$$ (Eq 012) $$W_{IN} = 20.48W \cdot 6.52ms = 0.13W \cdot s$$

Calculated input capacitor:

$$C_{INCal} = \frac{2 \cdot W_{IN}}{V^2_{DCMinPk} - V^2_{DCMinSet}}$$ (Eq 013) $$C_{INCal} = \frac{2 \cdot 0.13W \cdot s}{(120.2V)^2 - (93.2V)^2} = 46.35\mu F$$

Alternatively, a rule of thumb for estimating the input capacitor may be applied based on maximum input power, as shown below:

Input voltage	Factor
115 V AC	2 µF/W
230 V AC	1 µF/W
85–265 V AC	2–3 µF/W

Applying the rule of thumb using the 2 µF/W factor:

$$C_{INEst} = P_{INMax} \cdot factor \quad \textbf{(Eq 014)} \quad C_{INEst} = 20.48 \cdot 2\mu = 41\mu F$$

Choose a capacitance greater than or equal to calculated (Eq 013) or estimated (Eq 014) value, whichever is greater. The voltage rating should be greater than or equal to the maximum DC input voltage.

Input capacitor	C_{IN}	47 µF/500 V

Recalculation after input capacitor selection:

$$V_{DCMin} = \sqrt{V_{DCMinPk}^2 - \frac{2 \cdot W_{IN}}{C_{IN}}} \quad \textbf{(Eq 015)} \quad V_{DCMin} = \sqrt{(120.2V)^2 - \frac{2 \cdot 0.13W \cdot s}{47\mu F}} = 93.63V$$

Note: *Special requirements for hold-up time, including cycle skip/drop-out, or other factors which affect the resulting minimum DC input voltage and capacitor discharging time is not considered above.*

8.4 Transformer design (T1)

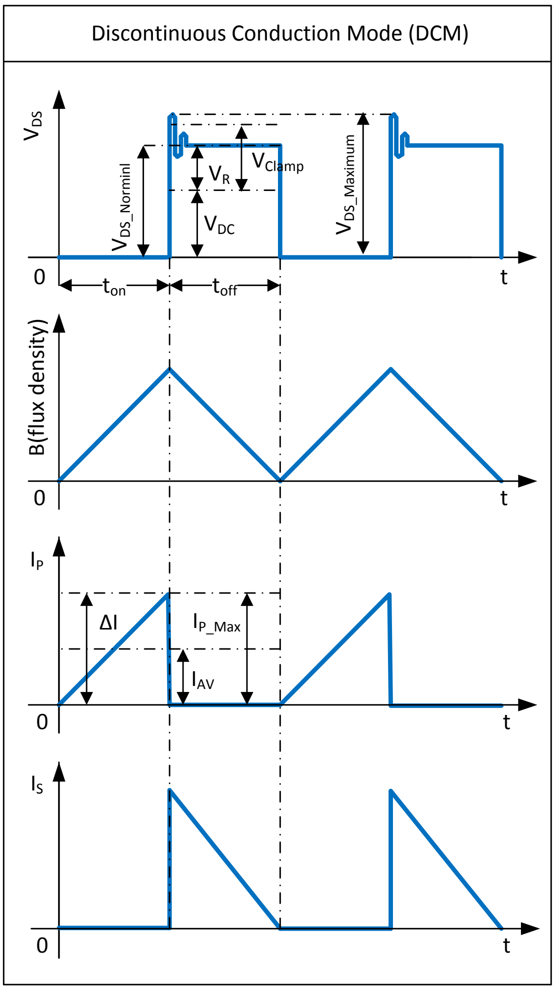

Figure 30 Typical waveforms of DCM operation

Maximum duty cycle:

$$D_{Max} = \frac{V_{RSET}}{V_{RSET} + V_{DCMin}} \quad \text{(Eq 016)} \quad D_{Max} = \frac{97.5V}{97.5V + 93.63V} = 0.51$$

Primary inductance:

$$L_P = \frac{(V_{DCMin} \times D_{Max})^2}{2 \times P_{InMax} \times f_s \times K_{RF}} \quad \text{(Eq 017)} \quad L_P = \frac{(93.63V \times 0.51)^2}{2 \times 20.48W \times 100kHz \times 1} = 556.7\mu H$$

Primary average current during turn-on:

$$I_{AV} = \frac{P_{InMax}}{V_{DCMin} \times D_{Max}} \quad \text{(Eq 018)} \quad I_{AV} = \frac{20.48W}{93.63V \times 0.51} = 0.43A$$

Primary peak-to-peak current:

$$\Delta I = \frac{V_{DCMin} \times D_{Max}}{L_P \times f_s} \quad \text{(Eq 019)} \quad \Delta I = \frac{93.63V \times 0.51}{556.7\mu H \times 100kHz} = 0.86A$$

Primary peak current:

$$I_{PMax} = I_{AV} + \frac{\Delta I}{2} \quad \text{(Eq 020)} \quad I_{PMax} = 0.43A + \frac{0.86A}{2} = 0.86A$$

Primary valley current:

$$I_{Valley} = I_{PMax} - \Delta I \quad \text{(Eq 021)} \quad I_{Valley} = 0.86A - 0.86A = 0A$$

Primary RMS current:

$$I_{PRMS} = \sqrt{[3 \times (I_{AV})^2 + (\frac{\Delta I}{2})^2] \times \frac{D\max}{3}} \quad \text{(Eq 022)} \quad I_{PRMS} = \sqrt{[3 \times (0.43)^2 + (\frac{0.86A}{2})^2] \times \frac{0.51}{3}} = 0.35A$$

Choose core type and bobbin from magnetics suppliers that can support the required power. Maximum flux density, typically from 200 mT to 400 mT, depends on the type of ferrite material. Below is the selected transformer material:

Core type	: E 20/10/6
Core material	: N87
Maximum flux density (B_S)	: 390 mT at 100°C
Cross-sectional area (A_e)	: 32 mm^2
Bobbin width (BW)	: 11 mm
Winding cross-section (A_N)	: 34 mm^2
Winding perimeter (l_N)	: 41.2 mm

Set maximum flux density | B_{MAX} | 200 mT

Calculate minimum primary number of turns:

$$N_{PCal} \geq \frac{I_{PMax} \cdot L_p}{B_{Max} \cdot A_e} \quad \text{(Eq 023)} \quad N_{PCal} \geq \frac{0.86A \times 556.7\mu H}{200mT \times 32mm^2} = 74.6Turns$$

Primary number of turns | N_P | 78 turns

Calculate secondary number of turns for V_{Out1}:

$$N_{S1Cal} = \frac{N_P \cdot (V_{Out1} + V_{FOut1})}{V_R} \quad \text{(Eq 024)} \quad N_{S1Cal} = \frac{78Turns \times (15V + 0.6V)}{97.5V} = 12.48Turns$$

Secondary 1 number of turns | N_{S1} | 12 turns

Calculate secondary number of turns for V_{Out2}:

$$N_{S2Cal} = \frac{N_P \cdot (V_{Out2} + V_{FOut2})}{V_R} \quad \text{(Eq 025)} \quad N_{S2Cal} = \frac{78Turns \times (5V + 0.2V)}{97.5V} = 4.16Turns$$

Secondary 2 number of turns | N_{S2} | 4 turns

Calculate number of turns for V_{CC}:

$N_{VccCal} = \frac{N_P \cdot (V_{Vcc} + V_{FVcc})}{V_R}$	(Eq 026)	$N_{VccCal} = \frac{78Turns \times (14V + 0.6V)}{97.5V} = 11.7Turns$
Auxiliary number of turns	N_{Vcc}	11 turns

Auxiliary supply voltage:

$V_{VccCal} = (V_{Out1} + V_{FOut1}) \cdot N_{Vcc} / N_{S1} - V_{FVcc}$	(Eq 027)	$V_{VccCal} = (15V + 0.6V) \cdot 11/12 - 0.6V = 13.7V$

8.5 Post calculation

Primary to secondary 1 turns ratio:

$N_{PS1} = N_P / N_{S1}$	(Eq 028)	$N_{PS1} = 78turns / 12turns = 6.5$

Primary to secondary 2 turns ratio:

$N_{PS2} = N_P / N_{S2}$	(Eq 029)	$N_{PS2} = 78turns / 4turns = 19.5$

Post-calculated reflected voltage:

$V_{RPost} = (V_{Out1} + V_{FOut1}) \cdot N_P / N_{S1}$	(Eq 030)	$V_{RPost} = (15V + 0.6V) \cdot 78/12 = 101.4V$

Post-calculated maximum duty cycle:

$D_{MaxPost} = \frac{V_{RPost}}{V_{RPost} + V_{DCMin}}$	(Eq 031)	$D_{MaxPost} = \frac{101.4V}{101.4V + 93.63V} = 0.52$

Duty cycle prime:

$D'_{Max} = \frac{L_P \cdot f_s \cdot (I_{PMax} - I_{Valley})}{V_{RPost}}$	(Eq 032)	$D'_{Max} = \frac{556.7\mu H \cdot 100kHz \cdot (0.86A - 0A)}{101.4V} = 0.47$

Actual flux density:

$B_{MaxAct} = \frac{L_P \cdot I_{PMax}}{N_P \cdot A_e}$	(Eq 033)	$B_{MaxAct} = \frac{556.7\mu H \cdot 0.86A}{78 \cdot 32mm^2} = 191mT$

Maximum DC input voltage for CCM operation:

$V_{DC\max CCM} = \left(\frac{1}{\sqrt{2 \cdot P_{InMax} \cdot L_P \cdot f_s}} - \frac{1}{V_{RPost}} \right)^{-1}$	(Eq 034)	$V_{DC\max CCM} = \left(\frac{1}{\sqrt{2 \cdot 20.48W \cdot 557\mu H \cdot 100kHz}} - \frac{1}{101.4V} \right)^{-1} = 90.3V$

8.6 Transformer winding design

Transformer design plays a big role in efficiency. Interlacing primary and output windings can reduce leakage inductance, and this is one way to improve efficiency. It is also critical for safety concerns, especially in isolated applications. Therefore, creepage and clearance should also be given serious consideration.

Standard safety margins between primary and secondary winding:

M = 4 mm for European safety standard
M = 3.2 mm for UL1950
M = 0 mm for triple-insulated wire on either primary or secondary winding

Standard safety margin	M	0 mm
Copper space factor	f_{Cu}	0.4 (0.2–0.4)

Effective bobbin width:

$$BW_E = BW - (2 \times M) \quad \text{(Eq 035)} \quad BW_E = 11mm - (2 \times 0) = 11mm$$

Effective winding cross-section:

$$A_{Ne} = \frac{A_N \times BW_e}{BW} \quad \text{(Eq 036)} \quad A_{Ne} = \frac{34mm^2 \times 11mm}{11mm} = 34mm^2$$

The effective winding cross-section must be divided between the primary and secondary windings. The design example is divided as follows:

Winding	Factor
Primary winding (AF_{NP})	50 %
Secondary winding 1(AF_{NS1})	30 %
Secondary winding 2 (AF_{NS2})	15 %
Auxiliary winding (AF_{NVcc})	5 %

8.6.1 Primary winding

Calculate copper wire cross-sectional area:

$$A_{PCal} = \frac{AF_{NP} \times f_{Cu} \times A_{Ne}}{N_P} \quad \text{(Eq 037)} \quad A_{PCal} = \frac{0.5 \times 0.4 \times 34mm^2}{78} = 0.087mm^2$$

Calculate maximum wire size:

$$AWG_{PCal} = 9.97 \cdot \left(1.8277 - \left(2 \cdot \log\left(2 \cdot \sqrt{\frac{A_{PCal}}{\pi}}\right)\right)\right) \quad \text{(Eq 038)} \quad AWG_{PCal} = 9.97 \cdot \left(1.8277 - \left(2 \cdot \log\left(2 \cdot \sqrt{\frac{0.087}{\pi}}\right)\right)\right) = 28$$

Selected wire size	AWG_P	30
Number of parallel wires	n_P	1

Copper wire diameter:

$$d_P = 10^{\left(\frac{1.8277}{2} - \frac{AWG_P}{2 \cdot 9.97}\right)} \quad \text{(Eq 039)} \quad d_P = 10^{\left(\frac{1.8277}{2} - \frac{30}{2 \cdot 9.97}\right)} = 0.26mm$$

Copper wire cross-sectional area:

$A_P = \frac{\pi}{4} \cdot d_P{}^2 \cdot n_p$	(Eq 040)	$A_P = \frac{\pi}{4} \cdot (0.26mm)^2 \cdot 1 = 0.0517mm^2$

Wire current density:

$S_P = \frac{I_{PRMS}}{A_P}$	(Eq 041)	$S_P = \frac{0.35A}{0.052mm^2} = 6.8A/mm^2$

Note: Recommended wire current density is less than 8 A/mm².

Number of turns per layer using INS = 0.01 mm:

$NL_P = \frac{BW_E}{n_P \cdot (d_P + 2 \cdot INS)}$	(Eq 042)	$NL_P = \frac{11mm}{1 \cdot (0.26mm + 2 \cdot 0.01mm)} = 39Turns/layer$

Note: Insulation thickness (INS) for single-, double- and triple-insulated wire is 0.01, 0.02 and 0.04 mm respectively. Ask the magnetics supplier for the actual insulation thickness.

Number of layers:

$Ln_P = N_p / NL_P$	(Eq 043)	$Ln_P = 78Turns/(39Turns/layer) = 2layers$

8.6.2 Secondary 1 winding (V_{Out1})

Calculate copper wire cross-sectional area:

$A_{NS1Cal} = \frac{AF_{NS1} \times f_{Cu} \times A_{Ne}}{N_{S1}}$	(Eq 044)	$A_{NS1Cal} = \frac{0.30 \times 0.4 \times 34mm^2}{12} = 0.34mm^2$

Calculate maximum wire size:

$AWG_{NS1Cal} = 9.97 \cdot \left(1.8277 - \left(2 \cdot \log\left(2 \cdot \sqrt{\frac{A_{NS1Cal}}{\pi}}\right)\right)\right)$	(Eq 045)	$AWG_{NS1Cal} = 9.97 \cdot \left(1.8277 - \left(2 \cdot \log\left(2 \cdot \sqrt{\frac{0.34mm^2}{\pi}}\right)\right)\right) = 22$
Selected wire size	AWG_{S1}	26
Number of parallel wires	n_{S1}	2

Copper wire diameter:

$d_{S1} = 10^{\left(\frac{1.8277}{2} - \frac{AWG_{S1}}{2 \cdot 9.97}\right)}$	(Eq 046)	$d_{S1} = 10^{\left(\frac{1.8277}{2} - \frac{26}{2 \cdot 9.97}\right)} = 0.407mm$

Copper wire cross-sectional area:

$A_{S1} = \frac{\pi}{4} \cdot d_{S1}{}^2 \cdot n_{S1}$	(Eq 047)	$A_{S1} = \frac{\pi}{4} \cdot (0.407)^2 \cdot 2 = 0.261mm^2$

Peak current:

$I_{S1Max} = I_{PMax} \cdot K_{L1} \cdot N_{PS1}$	(Eq 048)	$I_{S1Max} = 0.86A \cdot 0.86 \cdot 6.5 = 4.8A$

RMS current:

$I_{S1RMS} = I_{PRMS} \cdot K_{L1} \cdot \sqrt{\frac{1-D_{MaxPost}}{D_{MaxPost}}} \cdot N_{PS1}$	(Eq 049)	$I_{S1RMS} = 0.35A \cdot 0.86 \cdot \sqrt{\frac{1-0.52}{0.52}} \cdot 6.5 = 1.9A$

Wire current density:

$S_{S1} = \frac{I_{S1RMS}}{A_{S1}}$	(Eq 050)	$S_{S1} = \frac{1.9A}{0.261mm^2} = 7.3A/mm^2$

Number of turns per layer using INS = 0.01 mm (non-isolated design does not need triple-insulated wire):

$NL_{S1} = \left\lfloor \frac{BW_E}{nw_{S1} \cdot (d_{S1} + 2 \cdot INS_{S1})} \right\rfloor$	(Eq 051)	$NL_{S1} = \left\lfloor \frac{11mm}{2 \cdot (0.407mm + 2 \cdot 0.01mm)} \right\rfloor = 12Turns/layer$

Number of layers of secondary 1 winding:

$Ln_{S1} = \lceil N_{S1} / NL_{S1} \rceil$	(Eq 052)	$Ln_{S1} = \lceil 12Turns/(12Turns/layer) \rceil = 1layers$

8.6.3 Secondary 2 winding (V_{Out2})

Calculate copper wire cross-sectional area:

$A_{NS2Cal} = \frac{AF_{NS2} \times f_{Cu} \times A_{Ne}}{N_{S2}}$	(Eq 053)	$A_{NS2Cal} = \frac{0.15 \times 0.4 \times 34mm^2}{4} = 0.51mm^2$

Calculate maximum wire size:

$AWG_{NS2Cal} = 9.97 \cdot \left(1.8277 - \left(2 \cdot \log\left(2 \cdot \sqrt{\frac{A_{NS2Cal}}{\pi}}\right)\right)\right)$	(Eq 054)	$AWG_{NS2Cal} = 9.97 \cdot \left(1.8277 - \left(2 \cdot \log\left(2 \cdot \sqrt{\frac{0.34}{\pi}}\right)\right)\right) = 20$
Selected wire size	AWG_{S2}	26
Number of parallel wires	n_{S2}	1

Copper wire diameter:

$d_{S2} = 10^{\left(\frac{1.8277}{2} - \frac{AWG_{S2}}{2 \cdot 9.97}\right)}$	(Eq 055)	$d_{S2} = 10^{\left(\frac{1.8277}{2} - \frac{26}{2 \cdot 9.97}\right)} = 0.407mm$

Copper wire area:

$A_{S2} = \frac{\pi}{4} \cdot d_{S2}^{\ 2} \cdot n_{S2}$	(Eq 056)	$A_{S2} = \frac{\pi}{4} \cdot (0.407)^2 \cdot 1 = 0.13mm^2$

Peak current:

$I_{S2Max} = I_{PMax} \cdot K_{L2} \cdot N_{PS2}$	(Eq 057)	$I_{S2Max} = 0.86A \cdot 0.14 \cdot 19.5 = 2.3A$

RMS current:

$I_{S2RMS} = I_{PRMS} \cdot K_{L2} \cdot \sqrt{\frac{1-D_{MaxPost}}{D_{MaxPost}}} \cdot N_{PS2}$	**(Eq 058)**	$I_{S2RMS} = 0.35A \cdot 0.14 \cdot \sqrt{\frac{1-0.52}{0.52}} \cdot 19.5 = 0.9A$

Wire current density:

$S_{S2} = \frac{I_{S2RMS}}{A_{S2}}$	**(Eq 059)**	$S_{S2} = \frac{0.9A}{0.130mm^2} = 7A/mm^2$

Number of turns per layer using INS = 0.01 mm (non-isolated design does not need triple-insulated wire):

$NL_{S2} = \left\lfloor \frac{BW_E}{nw_{S2} \cdot (d_{S2} + 2 \cdot INS_{S2})} \right\rfloor$	**(Eq 060)**	$NL_{S2} = \left\lfloor \frac{11mm}{1 \cdot (0.407mm + 2 \cdot 0.01mm)} \right\rfloor = 25 Turns/layer$

Number of layers:

$Ln_{S2} = \lceil N_{S2} / NL_{S2} \rceil$	**(Eq 061)**	$Ln_{S2} = \lceil 4 Turns / 25 Turns/layer \rceil = 1 layer$

8.7 Clamping network

For calculating the clamping network, it is necessary to know the leakage inductance L_{LK}. The most common approach is to have the L_{LK} value given in a percentage of the L_p. If it is known that the transformer construction is consistent, the L_{LK} can be measured by shorting the secondary windings (assuming the availability of a good LCR meter).

Leakage inductance:

Leakage inductance percentage	$L_{LK\%}$	2.5 %
$L_{LK} = L_{LK\%} \cdot L_P$	**(Eq 062)**	$L_{LK} = 2.5\% \times 556.7\mu H = 13.9\mu H$

Clamping voltage:

$V_{Clamp} = V_{DSMax} - V_{DCMaxPk} - V_{RPost}$	**(Eq 063)**	$V_{Clamp} = 700V - 466.7V - 101.4V = 131.9V$

Calculate clamping capacitor:

$C_{ClampCal} = \frac{I_{PMax}^2 \cdot L_{LK}}{(V_{RPost} + V_{Clamp}) \cdot V_{Clamp}}$	**(Eq 064)**	$C_{ClampCal} = \frac{(0.86A)^2 \times 13.9\mu H}{(101.4V + 131.9V) \times 131.9V} = 334pF$
Clamping capacitor	C_{Clamp}	1 nF

Calculate clamping resistor:

$R_{ClampCal} = \frac{(V_{Clamp} + V_{RPost})^2 - V_{RPost}^2}{0.5 \cdot L_{LK} \cdot I_{PMax}^2 \cdot f_S}$	**(Eq 065)**	$R_{ClampCal} = \frac{(131.9V + 101.4V)^2 - (101.4V)^2}{0.5 \times 13.9\mu H \times (0.86A)^2 \times 100kHz} = 86k\Omega$
Clamping resistor	R_{Clamp}	68 kΩ

8.8 CS resistor

The CS resistor value defines the peak current of the power MOSFET. Therefore, the transformer should be designed not to saturate at this peak current value. Because the IC cycle-by-cycle PCL is defined by this resistor, it also defines the maximum output power that can be delivered.

CS resistor:

PCL threshold	V_{CS_N}	0.8 V
$R_{Sense}=\dfrac{V_{CS\_N}}{I_{PMax}}$	**(Eq 066)**	$R_{Sense}=\dfrac{0.8V}{0.86A}=0.93\Omega$

8.9 Output rectifier

A low forward voltage and an ultrafast diode such as a Schottky diode are recommended for a highly efficient design. These diodes are subjected to large peak and RMS current stress. The minimum voltage rating (not including voltage spikes) and minimum current rating (not including peak power transients) are calculated below.

The output capacitor is necessary to minimize the output ripple. It also holds the necessary energy needed during high load jumps. Therefore, the output capacitor should have enough capacitance and low ESR. It should also meet the ripple current rating.

An LC filter can be added to further reduce the output ripple.

8.9.1 Output 1

Diode reverse voltage:

$V_{RDiode1}=V_{Out1}+\left(\dfrac{V_{DCMaxPK}}{N_{PS1}}\right)$	**(Eq 067)**	$V_{RDiode1}=15V+\left(\dfrac{466.7V}{6.5}\right)=86.8V$
Diode RMS current	I_{S1RMS}	1.9 A

Output capacitor ripple current:

Maximum voltage undershoot	ΔV_{Out1}	0.3 V
Number of clock periods	n_{CP1}	20
$I_{Ripple1}=\sqrt{(I_{S1RMS})^2-(I_{Out1})^2}$	**(Eq 068)**	$I_{Ripple1}=\sqrt{(1.9A)^2-(0.83A)^2}=1.71A$

Calculated output capacitance:

$C_{Out1Cal}=\dfrac{I_{Out1}\cdot n_{CP1}}{\Delta V_{OUT1}\cdot f_S}$	**(Eq 069)**	$C_{Out1Cal}=\dfrac{0.83A\cdot 20}{0.3V\cdot 100kHz}=553\mu F$
Output capacitor	C_{Out1}	680 µF
ESR	R_{ESR1}	32 mΩ
Number of output capacitors in parallel	nc_{COut1}	1

Zero-frequency output capacitor:

$f_{ZCOut1} = \frac{1}{2 \cdot \pi \cdot R_{ESR1} \cdot C_{Out1}}$	(Eq 070)	$f_{ZCOut1} = \frac{1}{2 \cdot \pi \cdot 32m\Omega \cdot 680\mu F} = 7.3kHz$
Ripple voltage of first stage:		
$V_{Ripple1} = \frac{I_{S1Max} \cdot R_{ESR1}}{nc_{Cout1}}$	(Eq 071)	$V_{Ripple1} = \frac{4.8A \cdot 32m\Omega}{1} = 0.15V$

Calculated LC filter capacitor:

Select LC filter inductor	L_{Out1}	2.2 µH
$C_{LCCal1} = \frac{(C_{Out1} \cdot R_{ESR1})^2}{L_{out1}}$	(Eq 072)	$C_{LCCal1} = \frac{(680\mu F \cdot 32m\Omega)^2}{2.2\mu H} = 215\mu F$
LC filter capacitor	C_{LC1}	680 µF

LC filter frequency:

$f_{LC1} = \frac{1}{2 \cdot \pi \cdot \sqrt{C_{LC1} \cdot L_{OUT1}}}$	(Eq 073)	$f_{LC1} = \frac{1}{2 \cdot \pi \cdot \sqrt{680\mu F \cdot 2.2\mu H}} = 4.1kHz$

Second stage ripple voltage:

$V_{2ndRipple1} = V_{Ripple1} \cdot \frac{\frac{1}{2 \cdot \pi \cdot f_s \cdot C_{LC1}}}{\frac{1}{2 \cdot \pi \cdot f_s \cdot C_{LC1}} + (2 \cdot \pi \cdot f_s \cdot L_{OUT1})}$	(Eq 074)	$V_{2ndRipple1} = 0.15V \cdot \frac{\frac{1}{2 \cdot \pi \cdot 100kHz \cdot 680\mu F}}{\frac{1}{2 \cdot \pi \cdot 100kHz \cdot 680\mu F} + (2 \cdot \pi \cdot 100kHz \cdot 2.2\mu H)} = 0.26mV$

8.9.2 Output 2

Diode reverse voltage:

$V_{RDiode2} = V_{Out2} + \left(\frac{V_{DCMaxPk}}{N_{PS2}}\right)$	(Eq 075)	$V_{RDiode2} = 5V + \left(\frac{466.7V}{19.5}\right) = 28.9V$
Diode RMS current	I_{S2RMS}	0.92 A

Output capacitor ripple current for V_{Out2}:

Maximum voltage undershoot (V_{Out2})	ΔV_{Out2}	0.15 V
Number of clock periods	n_{CP2}	20
$I_{Ripple2} = \sqrt{(I_{S2RMS})^2 - (I_{Out2})^2}$	(Eq 076)	$I_{Ripple2} = \sqrt{(0.92A)^2 - (0.4A)^2} = 0.83A$

Calculated output capacitance:

$C_{Out2} = \frac{I_{Out2} \cdot n_{CP2}}{\Delta V_{OUT2} \cdot f_S}$	(Eq 077)	$C_{Out2} = \frac{0.4A \cdot 20}{0.15V \cdot 100kHz} = 533\mu F$
Output capacitor	C_{Out2}	680 µF
ESR	R_{ESR2}	32 mΩ
Number of output capacitors in parallel	nc_{COut2}	1

Zero-frequency output capacitor:

$$f_{ZCOut2} = \frac{1}{2 \cdot \pi \cdot R_{ESR2} \cdot C_{Out2}} \quad \text{(Eq 078)} \quad f_{ZCOut2} = \frac{1}{2 \cdot \pi \cdot 32m\Omega \cdot 680\mu F} = 7.3kHz$$

Ripple voltage of first stage:

$$V_{Ripple2} = \frac{I_{S2Max} \cdot R_{ESR2}}{nc_{Cout2}} \quad \text{(Eq 079)} \quad V_{Ripple2} = \frac{2.31A \cdot 32m\Omega}{1} = 0.07V$$

Calculated LC filter capacitor:

Select LC filter inductor	L_{Out2}	2.2 µH
$C_{LCCal2} = \frac{(C_{Out2} \cdot R_{ESR2})^2}{L_{out2}}$	(Eq 080)	$C_{LCCal2} = \frac{(680\mu F \cdot 32m\Omega)^2}{2.2\mu H} = 215\mu F$
LC filter capacitor	C_{LC2}	330 µF

LC filter frequency:

$$f_{LC2} = \frac{1}{2 \cdot \pi \cdot \sqrt{C_{LC2} \cdot L_{OUT2}}} \quad \text{(Eq 081)} \quad f_{LC2} = \frac{1}{2 \cdot \pi \cdot \sqrt{330\mu F \cdot 2.2\mu H}} = 5.9kHz$$

Second stage ripple voltage:

$$V_{2ndRipple2} = V_{Ripple2} \cdot \frac{\frac{1}{2 \cdot \pi \cdot f_s \cdot C_{LC2}}}{\frac{1}{2 \cdot \pi \cdot f_s \cdot C_{LC2}} + (2 \cdot \pi \cdot f_s \cdot L_{OUT2})} \quad \text{(Eq 082)}$$

$$V_{2ndRipple2} = 0.07V \cdot \frac{\frac{1}{2 \cdot \pi \cdot 100kHz \cdot 330\mu F}}{\frac{1}{2 \cdot \pi \cdot 100kHz \cdot 330\mu F} + (2 \cdot \pi \cdot 100kHz \cdot 2.2\mu H)} = 0.26mV$$

8.10 V_{CC} diode and capacitor

Auxiliary diode reverse voltage:

$$V_{RDiodeVCC} = V_{VccCal} + \left(V_{DCMaxPk} \cdot \frac{N_{Vcc}}{N_P} \right) \quad \text{(Eq 083)} \quad V_{RDiodeVCC} = 13.7V + \left(466.7 \times \frac{11}{78} \right) = 79.5V$$

Calculate minimum V_{CC} capacitor:

Soft-start time from datasheet	t_{SS}	12 ms
$I_{VCC\_Charge3}$ from datasheet	$I_{VCC\_Charge3}$	3 mA
V_{VCC_ON} from datasheet	V_{VCC_ON}	16 V
V_{VCC_OFF} from datasheet	V_{VCC_OFF}	10 V
$C_{VccCal} > \frac{I_{VCC\_Charge3} \cdot t_{SS}}{V_{VCC\_ON} - V_{VCC\_OFF}}$	(Eq 084)	$C_{VccCal} > \frac{3mA \cdot 12ms}{16V - 10V} = 6\mu F$
Selected V_{CC} capacitor	C_{VCC}	22 µF

Start-up time:

V_{CC} short threshold from datasheet	V_{VCC_SCP}	1.1 V
$I_{VCC\_Charge1}$ from datasheet	$I_{VCC\_Charge1}$	0.2 mA

$$t_{StartUp} = \frac{V_{VCC\_SCP} \cdot C_{VCC}}{I_{VCC\_Charge1}} + \frac{(V_{VCC\_ON} - V_{VCC\_SCP}) \cdot C_{VCC}}{I_{VCC\_Charge3}}$$ (Eq 085)

$$t_{StartUp} = \frac{1.1V \cdot 22\mu F}{0.2mA} + \frac{(16V - 1.1V) \cdot 22\mu F}{3mA} = 230ms$$

8.11 Calculation of losses

Input diode bridge loss:

Diode bridge forward voltage — V_{FBR} — 1 V

$$P_{DIN} = I_{ACRMS} \cdot V_{FBR} \cdot 2$$ (Eq 086) $$P_{DIN} = 0.4A \cdot 1V \cdot 2 = 0.8W$$

Transformer copper loss:

Copper resistivity at 100°C — ρ_{100} — 0.0172 Ω·mm²/m

$$R_{PCu} = \frac{l_N \cdot N_P \cdot \rho_{100}}{A_P}$$ (Eq 087) $$R_{PCu} = \frac{41.2mm \cdot 78 \cdot 0.0172\Omega \cdot mm^2/m}{0.052mm^2} = 1068.5m\Omega$$

$$R_{S1Cu} = \frac{l_N \cdot N_{S1} \cdot \rho_{100}}{A_{S1}}$$ (Eq 088) $$R_{S1Cu} = \frac{41.2mm \cdot 12 \cdot 0.0172\Omega \cdot mm^2/m}{0.2602mm^2} = 32.6m\Omega$$

$$R_{S2Cu} = \frac{l_N \cdot N_{S2} \cdot \rho_{100}}{A_{S2}}$$ (Eq 089) $$R_{S1Cu} = \frac{41.2mm \cdot 4 \cdot 0.0172\Omega \cdot mm^2/m}{0.13mm^2} = 21.8m\Omega$$

$$P_{PCu} = I_{PRMS}^{\ 2} \cdot R_{PCU}$$ (Eq 090) $$P_{PCu} = (0.35A)^2 \cdot 1068.5m\Omega = 133.63mW$$

$$P_{S1Cu} = I_{S1RMS}^{\ 2} \cdot R_{S1CU}$$ (Eq 091) $$P_{S1Cu} = (1.9A)^2 \cdot 32.6m\Omega = 118mW$$

$$P_{S2Cu} = I_{S2RMS}^{\ 2} \cdot R_{S2CU}$$ (Eq 092) $$P_{S2Cu} = (0.92A)^2 \cdot 21.8m\Omega = 18mW$$

$$P_{Cu} = P_{PCu} \cdot P_{S1CU} \cdot P_{S2Cu}$$ (Eq 093) $$P_{Cu} = 133mW + 118mW + 18mW = 270mW$$

Output rectifier diode loss:

$$P_{Diode1} = I_{S1RMS} \cdot V_{FOut1}$$ (Eq 094) $$P_{Diode1} = 1.9A \cdot 0.6V = 1.14W$$

$$P_{Diode2} = I_{S2RMS} \cdot V_{FOut2}$$ (Eq 095) $$P_{Diode2} = 0.92A \cdot 0.2V = 0.18W$$

RCD clamper loss:

$$P_{Clamper} = \frac{1}{2} \cdot L_{LK} \cdot I_{PMax}^2 \cdot f_S \cdot \frac{V_{Clamp} + V_{RPost}}{V_{Clamp}}$$ (Eq 096) $$P_{Clamper} = \frac{1}{2} \cdot 13.9\mu H \cdot (0.86A)^2 \cdot 100kHz \cdot \frac{132V + 101.4V}{132V} = 0.91W$$

CS resistor loss:

$$P_{CS} = (I_{PRMS})^2 \cdot R_{CS}$$ (Eq 097) $$P_{CS} = (0.35A)^2 \cdot 0.93\Omega = 0.12W$$

MOSFET loss:

R_{DSON} at T_J = 125°C from datasheet	R_{DSON}	8.73 Ω
$C_{o(er)}$ from datasheet	$C_{o(er)}$	3.4 pF
External drain-to-source capacitance	C_{DS}	0 pF
$P_{SONMinAC}=\frac{1}{2}\cdot\left(C_{o(er)}+C_{DS}\right)\cdot(V_{DCMin}-V_{RPost})^2\cdot f_S$	(Eq 098)	$P_{SONMinAC}=\frac{1}{2}\cdot(3.4pF+0pF)\cdot(93.6V+101.4V)^2\cdot 100kHz=6.5mW$
$P_{condMinAC}=I_{PRMS}{}^2\cdot R_{DSON}$	(Eq 099)	$P_{condMinAC}=(0.35A)^2\cdot 8.73\Omega=1.092W$
$P_{MOSMinAC}=P_{SONMinAC}+P_{condMinAC}$	(Eq 100)	$P_{MOSMinAC}=6.5mW+1.092W=1.098W$
$P_{SONMaxAC}=\frac{1}{2}\cdot\left(C_{o(er)}+C_{DS}\right)\cdot(V_{DCMaxPk}-V_{RPost})^2\cdot f_S$	(Eq 101)	$P_{SONMaxAC}=\frac{1}{2}\cdot(3.4pF+0pF)\cdot(466.7V+101.4V)^2\cdot 100kHz=$
$P_{condMaxAC}=\frac{1}{3}\cdot R_{DSON}\cdot I_{PMax}^2\cdot\left(\frac{L_P\cdot I_{PMax}\cdot f_S}{V_{DCMaxPk}}\right)$	(Eq 102)	$P_{condMaxAC}=\frac{1}{3}\cdot 8.73\Omega\cdot(0.86A)^2\cdot\left(\frac{557\mu H\cdot 0.86A\cdot 100kHz}{466.7V}\right)=0.22W$
$P_{MOSMaxAC}=P_{SONMaxAC}+P_{condMaxAC}$	(Eq 103)	$P_{MOSMaxAC}=54.9mW+0.22W=0.27W$

Controller loss:

Controller current consumption	I_{VCC_Normal}	0.9 mA
$P_{Ctrl}=V_{VCCCal}\cdot I_{VCC\_Normal}$	(Eq 104)	$P_{Ctrl}=13.7V\cdot 0.9mA=12.3mW$

Total power loss:

$P_{losses}=P_{DIN}+P_{Cu}+P_{Diode1}+P_{Diode2}+P_{Clamper}+P_{CS}+P_{MOS}+P_{Ctrl}$	(Eq 105)	$P_{losses}=0.8+0.27+1.14+0.18+0.91+0.12+1.1+0.01=4.53W$

Efficiency after losses:

$\eta_{Post}=P_{OutMax}/(P_{OutMax}+P_{lossoes})$	(Eq 106)	$\eta_{Post}=17W/(17W+4.53W)=78.95\%$

8.12 CoolSET™/MOSFET temperature

CoolSET™/MOSFET temperature:

Assumed junction-to-ambient thermal impedance (include copper pour)	R_{thJA_As}	65 K/W
$\Delta T=R_{thJA\_As}\cdot P_{MOS}$	(Eq 107)	$\Delta T=65K/W\cdot 1.098W=71.4°K$
$T_{j\max}=\Delta T+T_{a\max}$	(Eq 108)	$T_{j\max}=71.4+50=121.4°C$

8.13 LOVP

LOVP:

Selected AC input LOVP	V_{OVP_AC}	330 V AC
High-side DC input voltage divider resistor (R3A, R3B, R3C)	R_{I1}	9 MΩ
Controller LOVP threshold	V_{VIN_LOVP}	2.85 V

$$R_{I2Cal} = \frac{R_{I1} \cdot V_{VIN\_LOVP}}{\left(V_{OVP\_AC} \cdot \sqrt{2} - V_{VIN\_LOVP}\right)}$$	(Eq 109)	$$R_{I2Cal} = \frac{9M\Omega \cdot 2.85V}{\left(330V_{AC} \cdot \sqrt{2} - 2.85V\right)} = 55.3\Omega$$
Select low-side DC input voltage divider resistor	R_{I2}	56 kΩ
$$V_{OVP\_ACPost} = \frac{V_{VIN\_LOVP}}{R_{I2}} \cdot \frac{R_{I1} + R_{I2}}{\sqrt{2}}$$	(Eq 110)	$$V_{OVP\_ACPost} = \frac{2.85V}{56k\Omega} \cdot \frac{9M\Omega + 56k\Omega}{\sqrt{2}} = 326V_{AC}$$

8.14 Output regulation (non-isolated)

Setting resistor dividers for two non-isolated outputs:

Error amplifier reference voltage	V_{ERR_REF}	1.8 V
Weighted regulation factor of V_{Out1}	W_1	31 %
Select voltage divider RO1	R_{O1}	39 kΩ
$$R_{O2Cal} = \frac{V_{Out1} - V_{ERR\_REF}}{W_1 \cdot V_{ERR\_REF} / R_{O1}}$$	(Eq 125)	$$R_{O2Cal} = \frac{15V - 1.8V}{31\% \cdot 1.8V / 39k\Omega} = 922k\Omega$$
Select voltage divider RO2	R_{O2}	910 kΩ
$$R_{O3Cal} = \frac{V_{Out2} - V_{ERR\_REF}}{\frac{V_{ERR\_REF}}{R_{O1}} - \frac{V_{Out1} - V_{ERR\_REF}}{R_{O2}}}$$	(Eq 126)	$$R_{O3Cal} = \frac{5V - 1.8V}{\frac{1.8V}{39k\Omega} - \frac{15V - 1.8V}{910k\Omega}} = 101k\Omega$$
Select voltage divider RO3	R_{O3}	100 kΩ

9 References

[1] ICE5xSAG datasheet, Infineon Techonologies AG

[2] ICE5xRxxxxAG datasheet, Infineon Techonologies AG

[3] AN_201702_PL83_005 60W 19V SMPS Demo Board with ICE5GSAG and IPA80R600P7

[4] ER_201708_PL83_016 14 W 15 V 5 V SMPS demo board with ICE5AR4770AG

[5] Flycal_FF_F5 CoolSET

Revision history

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