25 – 150 V Source-down technology in PQFN 3.3 x 3.3

Kevin Ream (IFAM PSS DCDC PD PMG BE)
December 2021

Table of contents

Table of contents

Why source-down?
- Innovation on Silicon technology is not enough

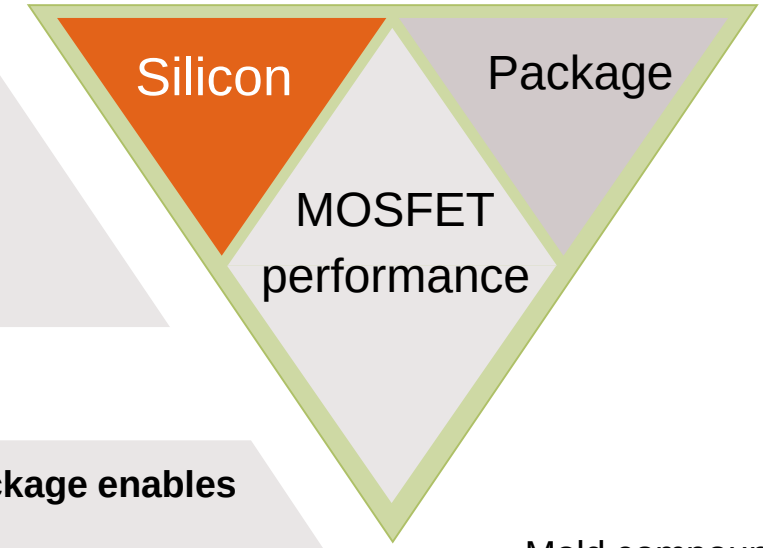
MOSFET performance is limited by two dimensions:

› Silicon technology

› Package limmitations

General trends in Power Management

1. Higher efficiency
2. Higher power density
3. BOM (Bill Of Material) cost reduction



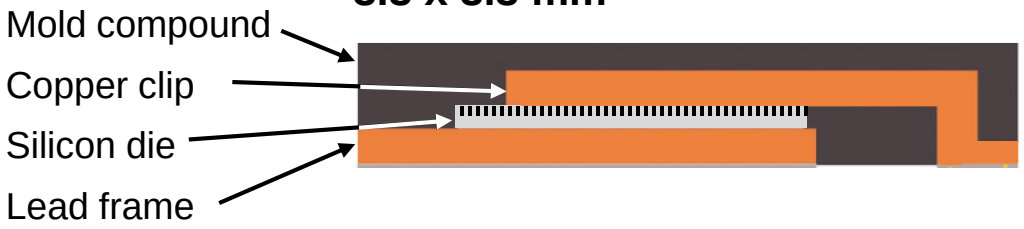
New source-down, industry standard package enables higher power density by:

› Lower $R_{DS(on)}$ in PQFN 3.3x3.3 mm^2 package-outline

› Improved thermal performance

› More effective layout for thermal management

Drain-down
3.3 x 3.3 mm



Drain-down vs. Source-down

Drain-down vs. Source-down

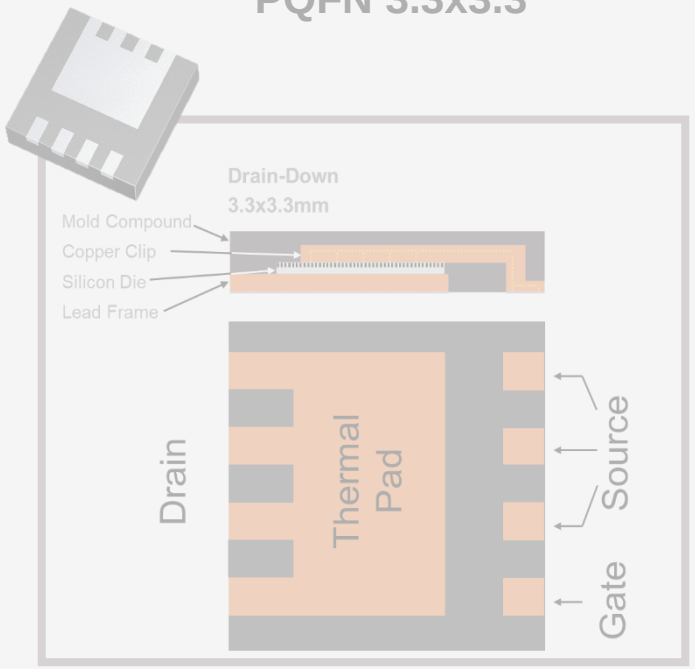
Silicon die is flipped upside-down

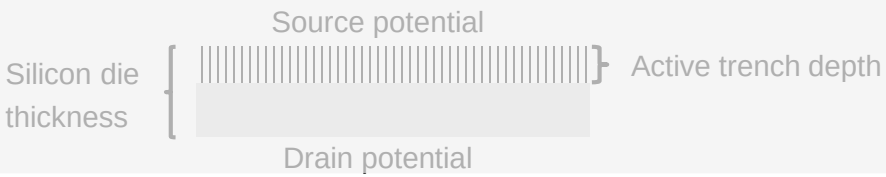
Active trenchnes on the silicon die are connected to lead frame

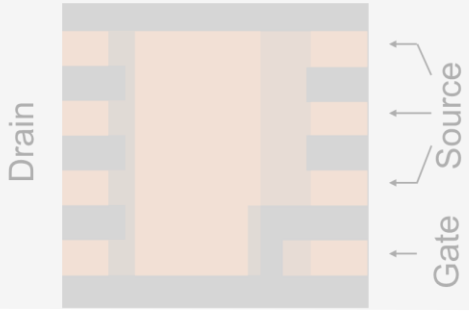
Thermal pad on source potential

Layout connections unchanged!*

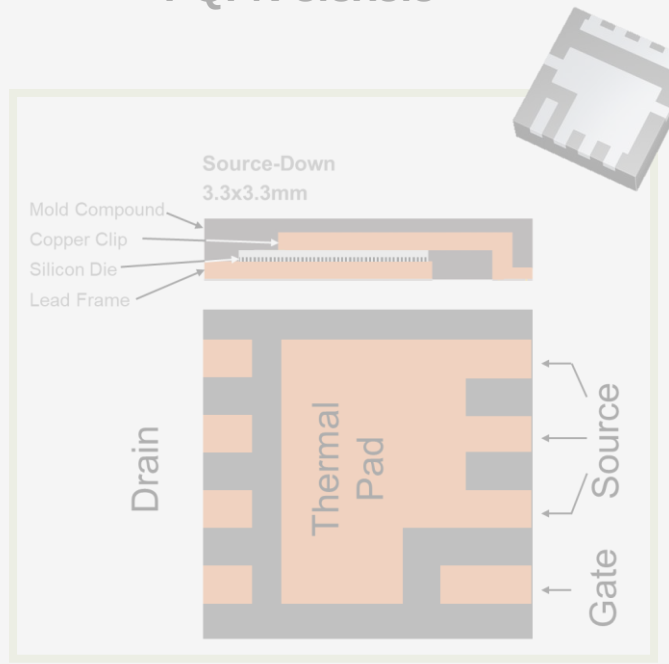
Drain-down
PQFN 3.3x3.3







Source-down
PQFN 3.3x3.3



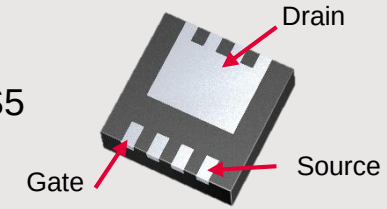
*Offering easy drop in replacement

Table of contents

Examples: standard drain-down vs. source-down

Drain-down

e.g. BSZ010NE2LS5 or BSZ009NE2LS5

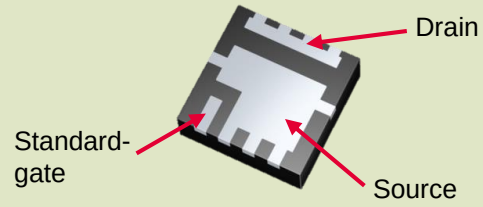


Features:

- PQFN 3.3 x 3.3 mm^2 package size
- Best in class $R_{DS(on)}$ and FOM
- BSZ010NE2LS5 $R_{DS(on)}$ = 1.0 mΩ
- BSZ009NE2LS5 $R_{DS(on)}$ = 0.9 mΩ (Or-ing optimized)

Source-down

e.g. IQE006NE2LM5



Features:

- PQFN 3.3 x 3.3 mm^2 package size
- **New best in class $R_{DS(on)}$ = 0.65 mΩ**
- High continuous (I_D=298 A) and pulse current (1192 A) capability
- Superior **thermal resistance R_{thJC} = 1.4°C/W** for source-down vs. 1.8°C/W for drain-down

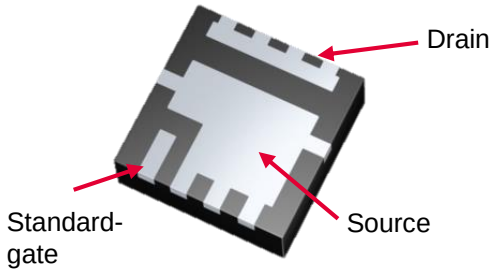
Parameter	BSZ009NE2LS5	BSZ010NE2LS5	IQE006NE2LM5	Unit
V_{DS}	25	25	25	V
$R_{DS(on),max}$	**0.9**	**1.0**	**0.65**	**mΩ**
R_{thJC}	1.8	1.8	1.4	°C/W
I_D	40	40	298	A
FOM_{Qg}	111.6	60.0	53.4	mΩ*nC

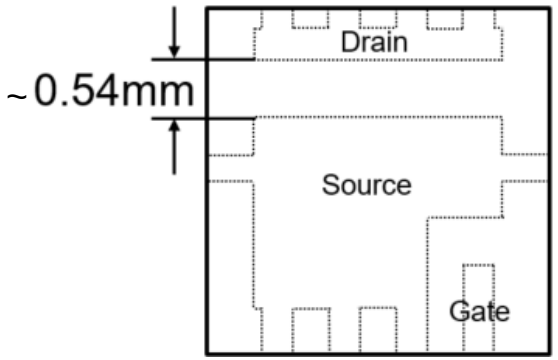
Source-down PQFN 3.3 x 3.3 mm² in 25 V

Source-down standard-gate vs. source-down center-gate

Source-down standard-gate (PG-TSON-8-4)

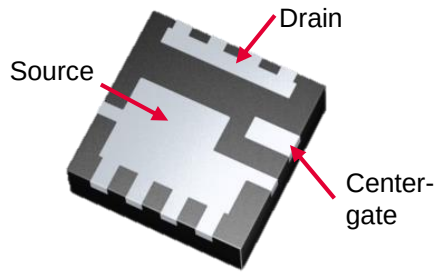
- Offering the source-down benefits
- Based on the existing PQFN 3.3 x 3.3 mm² pinout configuration
- Easy to adapt on existing PCB layout

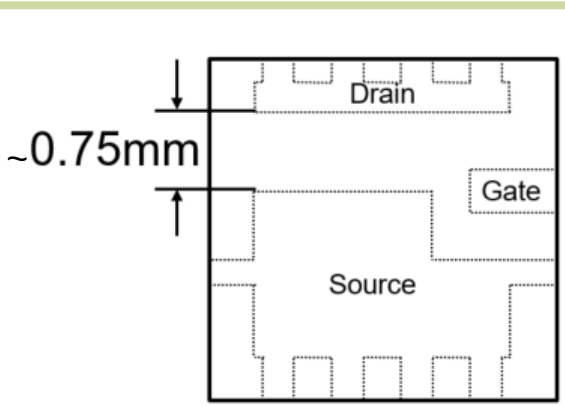




Source-down center-gate (PG-TTFN-9-1)

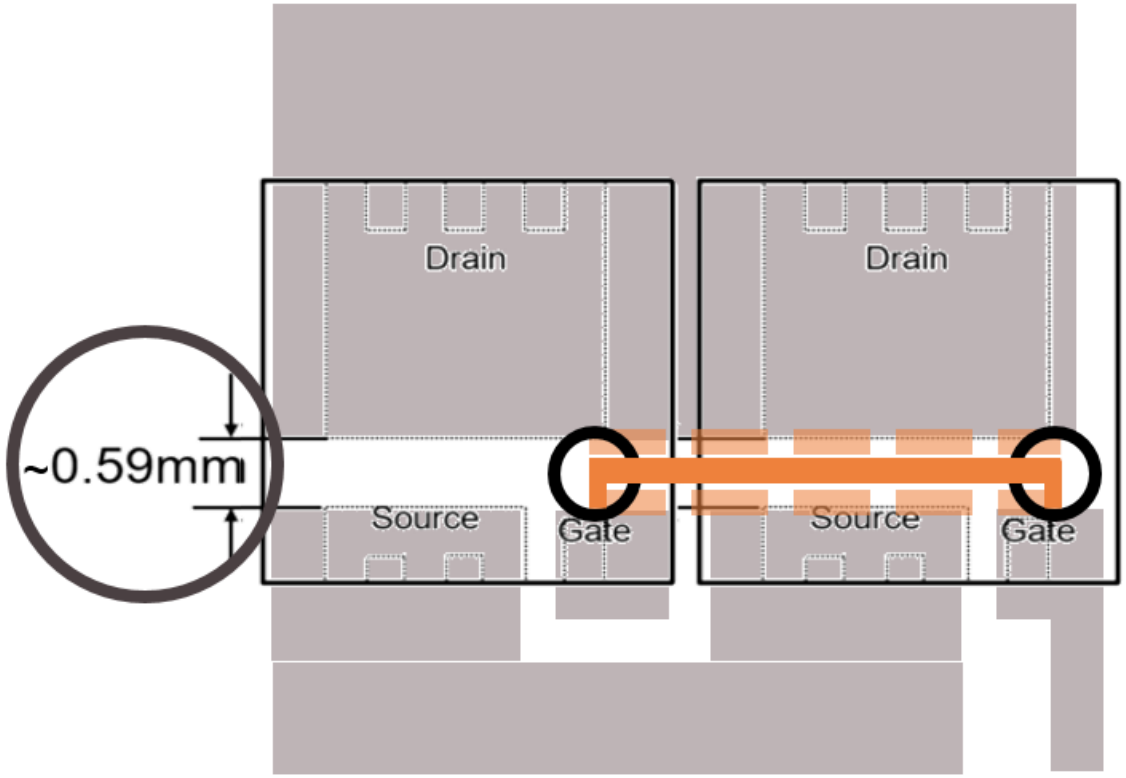
- Offering the source-down benefits
- Provides a layout option for **optimized parallelization** of MOSFETs
- Increased **source pad** improves connection area



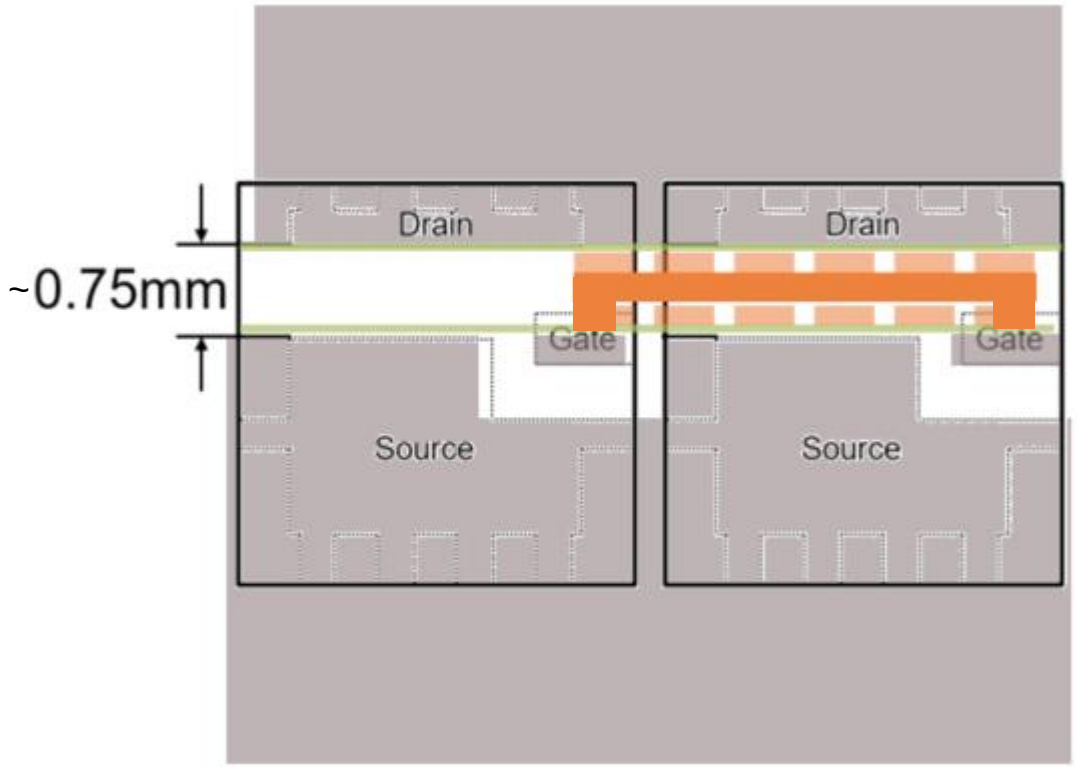


Drain-down vs. source-down center-gate parallelization comparison

Drain-down
Standard footprint parallelization
(PQFN 3.3x3.3)



Source-down footprint
Center-gate parallelization



Parallelization of MOSFETs

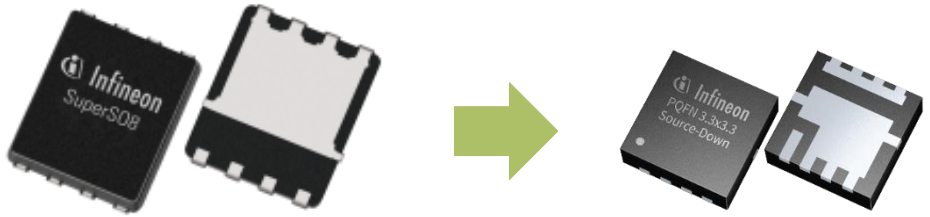
› The center-gate layout option enables easier paralleling with its larger drain to source creepage distance

Table of contents

Performance overview: lower $R_{DS(on)}$

Industry Benchmark in $R_{DS(on)}$) for small form factor

- **Reduction of $R_{DS(on)}$** up to 30% compared to SSO8 in 5x6 (BSC009NE2LS5)
- Lower I^2R losses
- **Significant shrink of form factor** / performance of a 5 x 6 mm^2 Super SO8 (PQFN) in only 3.3 x 3.3 mm^2
- More effective use of real estate
- Cooler design (less losses)



5 x 6 mm^2 3.3 x 3.3 mm^2

Part number	V_{DS}	Package	RDS(on) max @ 10 V_{GS}
BSC009NE2LS5	25	SS08 5x6	0.9 mΩ
IQE006NE2LM5		Source down 3x3	**0.65 mΩ**

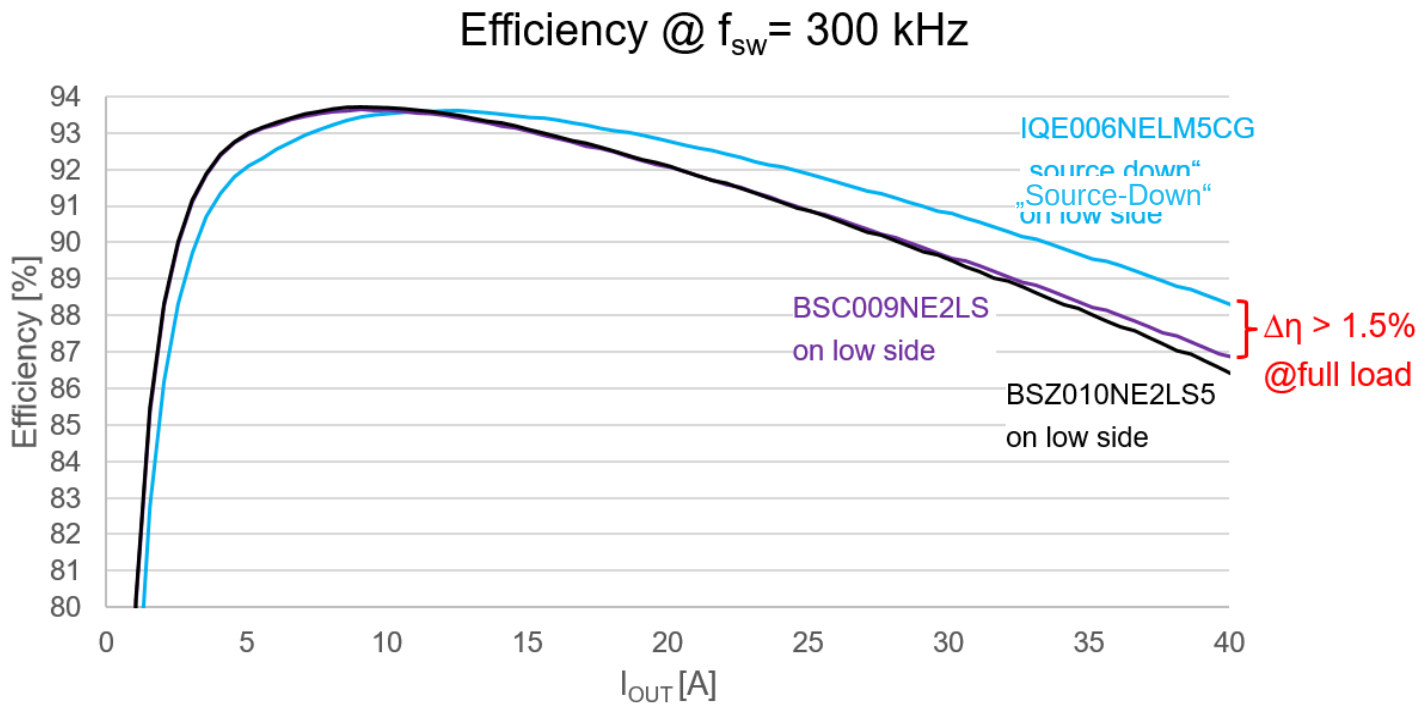
Improved power density and small form factor!!!!

Performance overview: efficiency

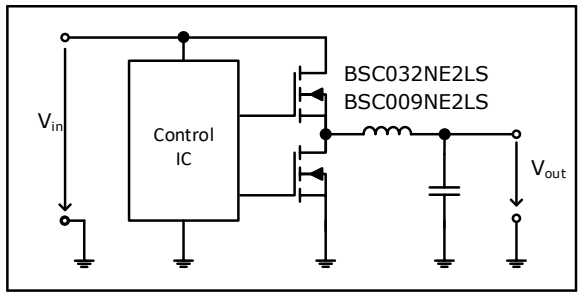
Efficiency benefits

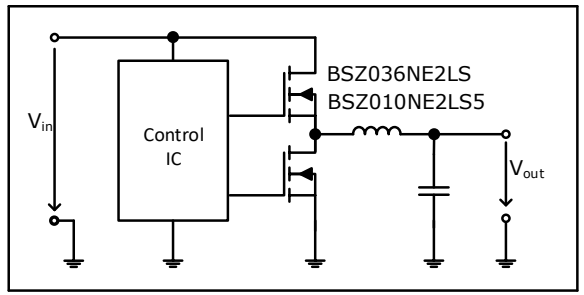
- Lower $R_{DS(on)}$
  - Limits the I^2R losses
- Lower package parasitics
  - Leads to better FOM
- Decreased R_{thJC}
  - Results in improved thermal behavior

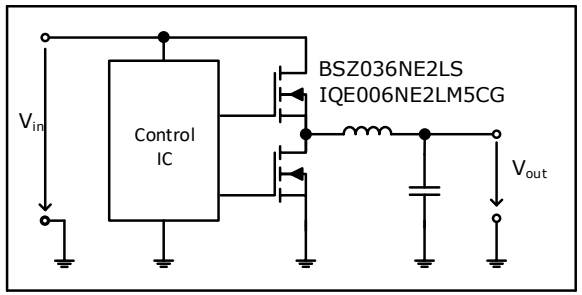
Higher efficiency!!



Efficiency measurments on Sync Buck converter @ 300 kHz







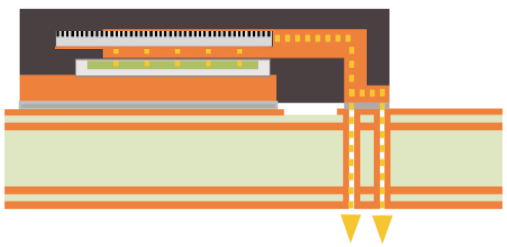
Performance overview: optimized thermal management

Optimized thermal management

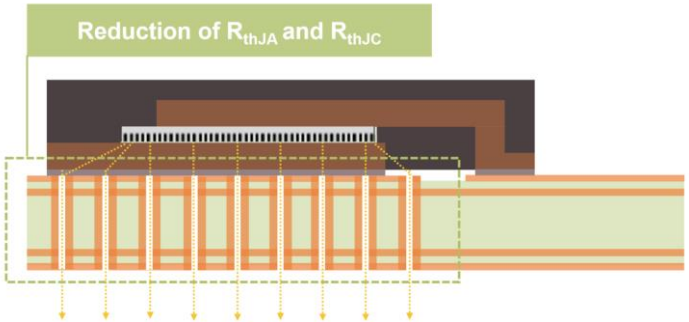
- **Source-down** concept enables direct connection of active area to leadframe => **reduction of R_{thJC}**
- Thermal pad is connected to source potential
  - Can be connected directly to the ground plane (i.e. for a low-side FET in a H-Bridge configuration)
  - Thermal vias can be used to connect to other layers => **Decrease of the R_{thJA} and R_{thJC}** (areas connected to GND does not need to be minimized)

Improved thermal capability!!

Normal drain-down
3.3 x 3.3 mm²



Source-down
3.3 x 3.3 mm²



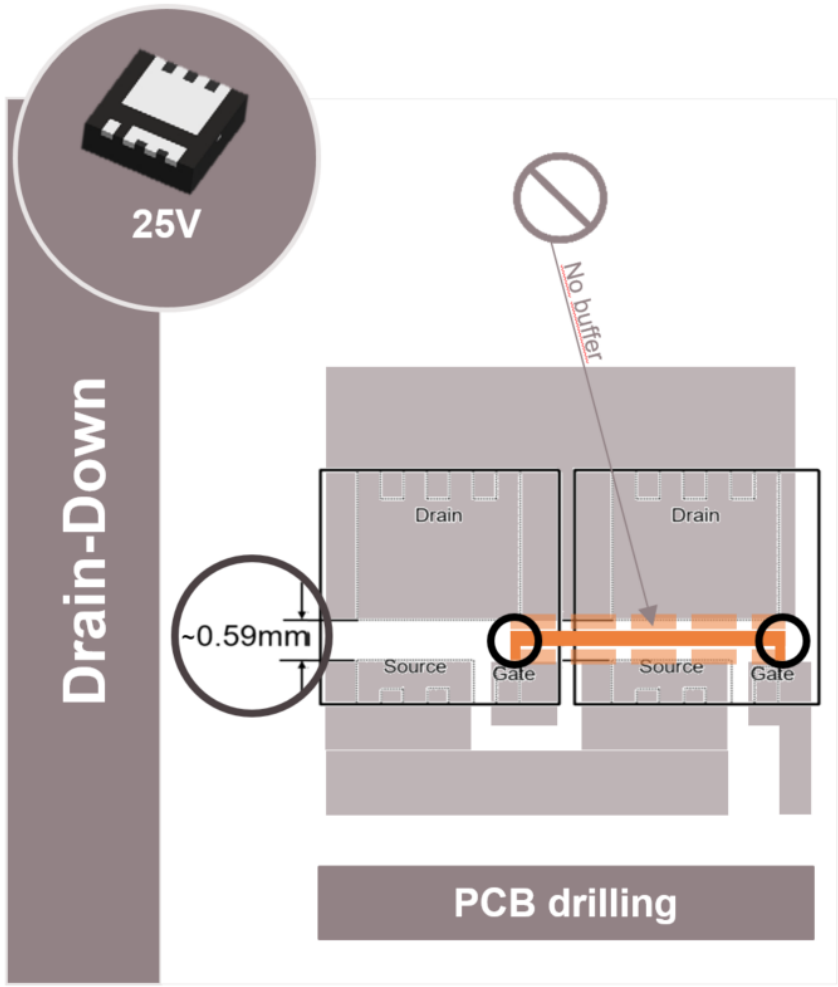
Heat can be sent efficiently into ground plains instead of switch node

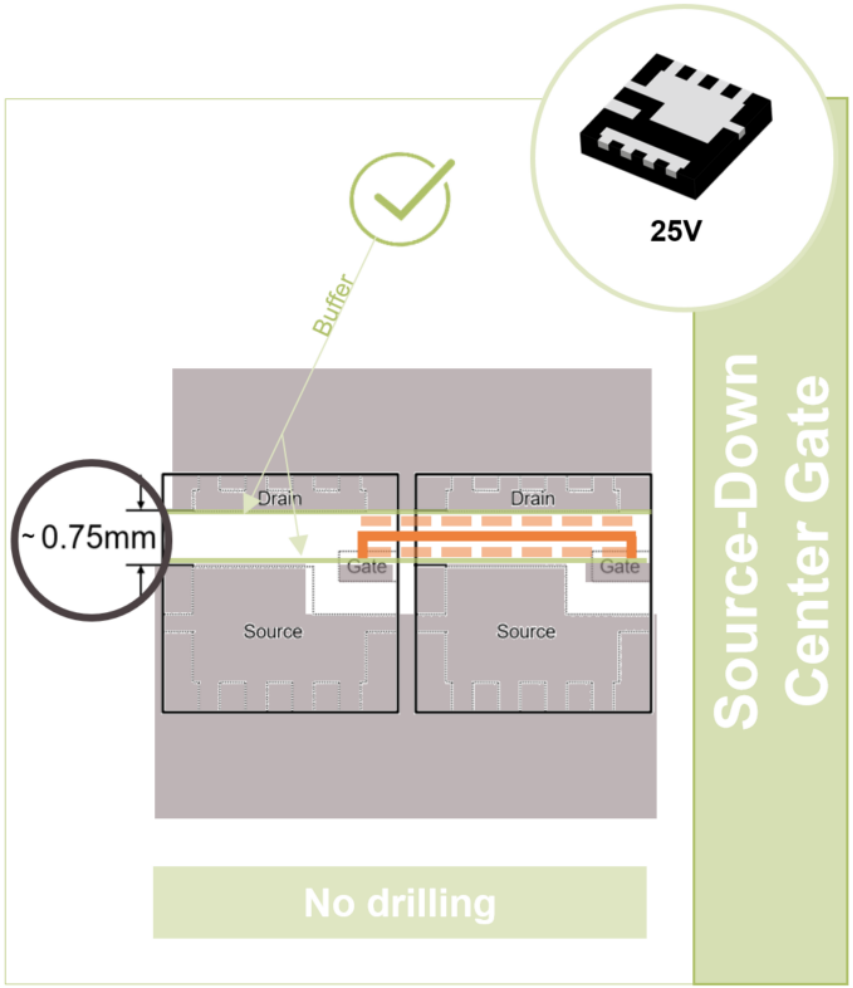
Performance overview: optimized layout

Layout comparison

- Layout is optimized for the parallelization of MOSFETs
- Easy and efficient parallelization
- Center-gate allows the connection of gates for paralleling on the same layer
- Same performance for source-down with 0.65 mOhm in 25 V compared to a 5x6 product -> board space is saved

Optimized layout possibilities!!





Performance overview: thermal performance

Thermal benefits

- Lower $R_{DS(on)}$ limits the I^2R losses
- Lower FOM Qg reduces switching losses
- Decreased R_{thJC} improves cooling behaviour

Better cooling possibilities!

cooler design

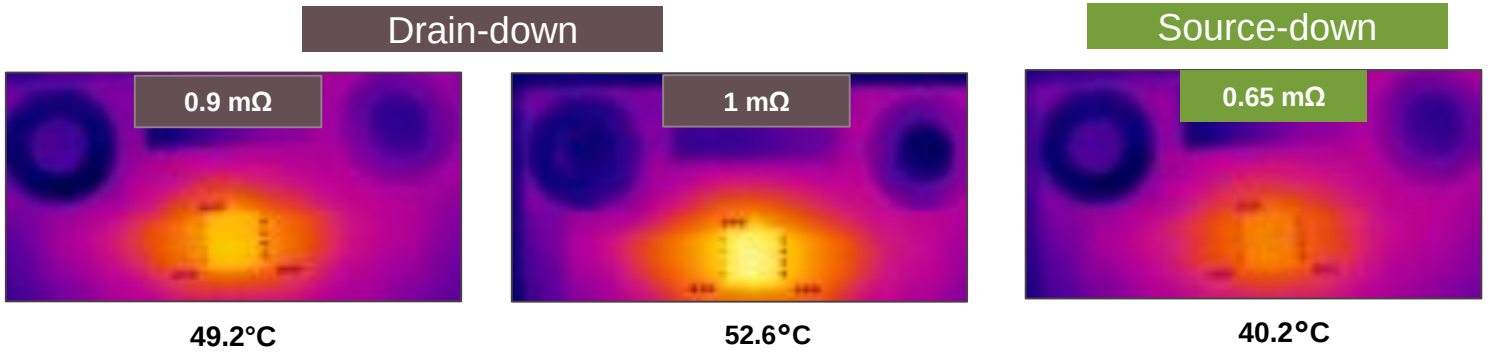
**measurements at 25°C, 30 A static current*

***thermal behavior of HSC at 450 W from 48 V input:*

a) with BSZ011NE2LS5I

b) with IQE006NE2LM5 ($T_{amb} = 24°C$ and $v = 3.3\ m/s$)

Thermal performance static switch*



Thermal performance Resonant DC-DC converter**

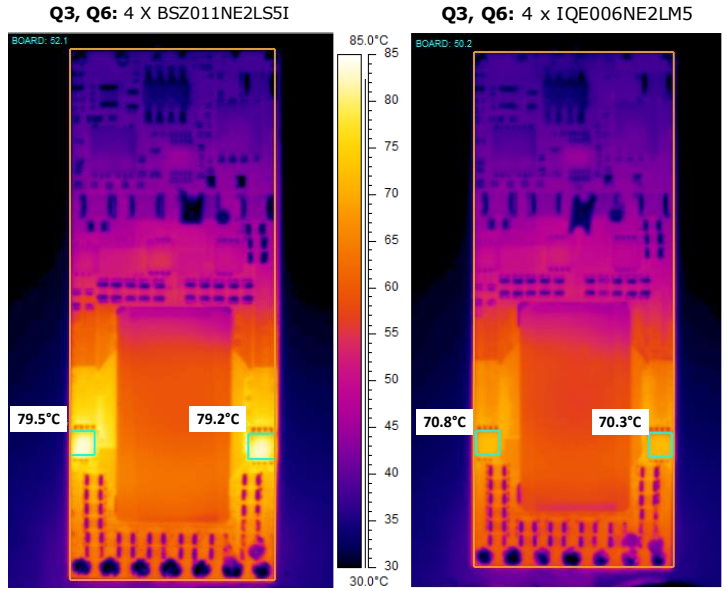
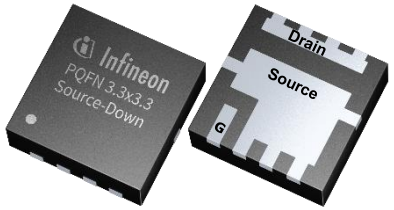
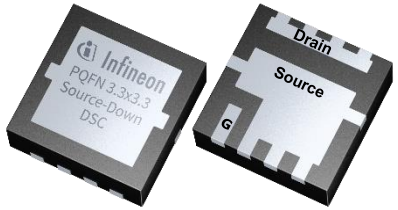
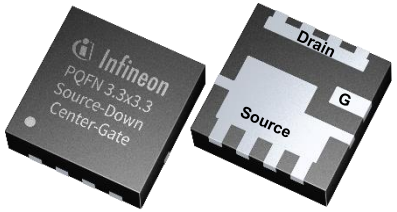
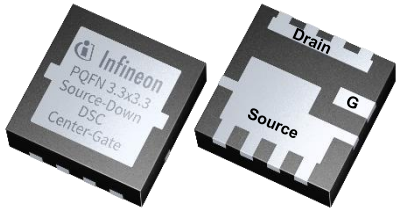


Table of contents

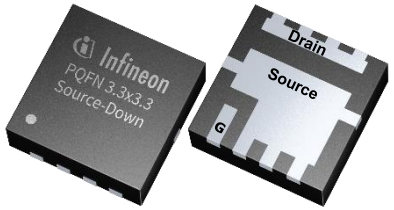
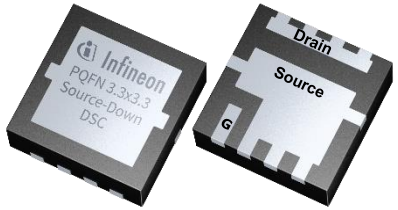
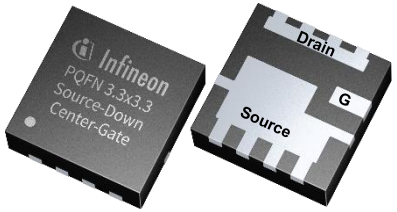
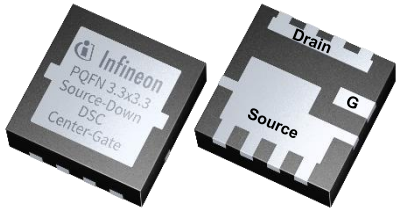
Initial Product Portfolio (Source-Down PQFN 3x3)
Target Release Schedule

		Standard Gate		Standard Gate DSC		Center-Gate		Center-Gate DSC	
				 Double-Side Cooling capabillity				 Double-Side Cooling capabillity	
Voltage Class	Target Rdson [mOhm]	Sales Name Standard gate	Target Release schedule	Sales Name Standard Gate DSC	Target Release schedule	Sales Name Center-Gate	Target Release schedule	Sales Name Center-Gate DSC	Target Release schedule
25V	≤0,6	IQE006NE2LM5	released	IQE006NE2LM5SC	Q3/CY2022	IQE006NE2LM5CG	released	IQE006NE2LM5CGSC	Q3/CY2022
30V	≤0,7	IQE008N03LM5	released	IQE008N03LM5SC	Q3/CY2022	IQE008N03LM5CG	released	IQE008N03LM5CGSC	Q3/CY2022
40V	≤1,3	IQE013N04LM6	released	IQE013N04LM6SC	Q3/CY2022	IQE013N04LM6CG	released	IQE013N04LM6CGSC	Q3/CY2022
60V	≤3,0	IQE030N06NM5	released	IQE030N06NM5SC	Q3/CY2022	IQE030N06NM5CG	released	IQE030N06NM5CGSC	Q3/CY2022
80V	≤6,0	IQE050N08NM5	released	IQE050N08NM5SC	Q3/CY2022	IQE050N08NM5CG	released	IQE050N08NM5CGSC	Q3/CY2022
100V	≤7,5	IQE065N10NM5	released	IQE065N10NM5SC	Q3/CY2022	IQE065N10NM5CG	released	IQE065N10NM5CGSC	Q3/CY2022
150V	≤22	IQE220N15NM5	Q2/CY2022	IQE220N15NM5SC	Q4/CY2022	IQE220N15NM5CG	Q2/CY2022	IQE220N15NM5CGSC	Q4/CY2022

Preliminary Information. Subject to change.

Press arrow to return to RM

Initial Product Portfolio (Source-Down PQFN 3x3)
Sample Schedule (Target)

		Standard gate		Standard Gate DSC		Center-Gate		Center-Gate DSC	
				 Double-Side Cooling capabillity				 Double-Side Cooling capabillity	
Voltage Class	Target Rdson [mOhm]	Sales Name Standard gate	ES Sample Schedule	Sales Name Standard Gate DSC	ES Sample Schedule	Sales Name Center-Gate	ES Sample Schedule	Sales Name Center-Gate DSC	ES Sample Schedule
25V	≤0,6	IQE006NE2LM5	avialalble	IQE006NE2LM5SC	avialalble	IQE006NE2LM5CG	avialalble	IQE006NE2LM5CGSC	avialalble
30V	≤0,7	IQE008N03LM5	avialalble	IQE008N03LM5SC	avialalble	IQE008N03LM5CG	avialalble	IQE008N03LM5CGSC	avialalble
40V	≤1,3	IQE013N04LM6	available	IQE013N04LM6SC	avialalble	IQE013N04LM6CG	avaialble	IQE013N04LM6CGSC	avialalble
60V	≤3,0	IQE030N06NM5	avialble	IQE030N06NM5SC	avialalble	IQE030N06NM5CG	avialalble	IQE030N06NM5CGSC	avialalble
80V	≤6,0	IQE050N08NM5	available	IQE050N08NM5SC	avialalble	IQE50XN08NM5CG	avaialble	IQE050N08NM5CGSC	avialalble
100V	≤8,0	IQE065N10NM5	available	IQE065N10NM5SC	available	IQE065N10NM5CG	available	IQE065N10NM5CGSC	avialalble
150V	≤22	IQE220N15NM5	available	IQE220N15NM5SC	availble	IQE220N15NM5CG	available	IQE220N15NM5CGSC	available

Preliminary Information. Subject to change.

Press arrow to return to RM

Value proposition & summary

Source-down concept of Infineon at a glance: improved thermal capability especially for low-side switches and lower R_{thJA}

Key features	Key benefits	Value
$R_{DS(on)}$ reduction up to 30% depending on the voltage class	› Decreased I^2R losses › Higher current capability › Highest power density and performance	Higher system efficiency
Optimized layout possibilities	› Same performance as Super SO8 in smaller package › Shrink of form factor › Optimized PCB parasitics	System form factor reduction
Superior thermal performance	› Decrease of R_{thJA} and R_{thJC} › Better transfer of power losses › Supports double side cooling (exposed clip)	More relaxed thermal management
Two footprint versions available	› Source-down is easy to adapt on existing PCB › Center-gate option enables optimized parallelization	Optimal device arrangement on the PCB

Easy to Use

Part of your life. Part of tomorrow.